

2018 IEEE Asian Solid-State Circuits Conference Technical Program

Day 1	November 5 (Monday)	
08:30 - 18:00	Registration (Foyer, B2F)	
09:00 - 10:30	Tutorial 1 When SAR Meets $\Delta\Sigma$ - A Tale of Two ADC Architectures - <u>Nan Sun</u> / University of Texas at Austin, USA (South+West+East Gate, B1F)	
10:30 - 10:50	Break	
10:50 - 12:20	Tutorial 2 Wireless ECG Acquisition and Cardiac Stimulation SOC's for Body Sensor Networks <u>Shuenn-Yuh Lee</u> / National Cheng Kung University, Taiwan (South+West+East Gate, B1F)	
12:20 - 13:40	Lunch	
13:40 - 15:10	Tutorial 3 Terahertz CMOS Technology for Beyond 5G <u>Minoru Fujishima</u> / Hiroshima University, Japan (South+West+East Gate, B1F)	
15:10 - 15:30	Break	
15:30 - 17:00	Tutorial 4 Memory System for Next Generation AI <u>Kyomin Sohn</u> / Samsung Electronics, Korea (South+West+East Gate, B1F)	
17:00 - 19:00	SDC Exhibition (Foyer, B1F)	FPGA Demo (Foyer, B1F)
18:00 - 19:30	Welcome Reception (Far Eastern Grand Ballroom A+B, B2F)	

Day 2	November 6 (Tuesday)					
07:45 - 18:00	Registration (Foyer, B2F)					
08:30 - 08:50	Opening Ceremony (Far Eastern Grand Ballroom A+B, B2F)					
08:50 - 09:35	Plenary Talk 1 Circuit Design in Nano-Scale CMOS Technologies Dr. Kevin Zhang / VP, Business Development, TSMC, Taiwan (Far Eastern Grand Ballroom A+B, B2F)					
09:40 - 10:25	Plenary Talk 2 Open the New World of 5G Mr. Seizo ONOE / CTA, NTT DOCOMO & President, DOCOMO Tech., Japan (Far Eastern Grand Ballroom A+B, B2F)					
10:25 - 10:50	Break					
10:50 - 12:30	Industry 2 Advanced Techniques for Industrial Applications (Far Eastern Grand Ballroom A+B, B2F)		ETA 3 Intelligent Sensor and Imager Systems (East Gate, B1F)		SDC Exhibition (Foyer, B1F)	FPGA Demo (Foyer, B1F)
12:30 - 13:30	Lunch					
13:30 - 15:10	ACS 4 Power Converters and Sensors (North Gate, B1F)	FPGA 5 FPGA-based AI Computing (South Gate, B1F)	WLN 6 Optical Link and CDR (West Gate, B1F)	RF 7 Millimeter-Wave Transceivers and Terahertz Sensors (East Gate, B1F)		
15:10 - 15:30	Break					
15:30 - 17:30	PD 8 : Panel Discussion (Far Eastern Grand Ballroom B, B2F)					
17:30 - 19:00	Break					
19:00 - 21:00	Banquet (Far Eastern Grand Ballroom A+B, B2F)					

Day 3	November 7 (Wednesday)			
07:45 - 12:00	Registration (Foyer, B2F)			
08:30 - 09:15	Plenary Talk 3 Practical Challenges in Supporting Functions in Memory <u>Dr. Nam Sung Kim</u> / SVP, Memory Division, Samsung, Korea (Far Eastern Grand Ballroom A+B, B2F)			
09:20 - 10:05	Plenary Talk 4 AI Drive Domain Specific Processor <u>Dr. Yi Kang</u> / Chief Scientist & SVP, UNISOC, China (Tsinghua Unigroup) (Far Eastern Grand Ballroom A+B, B2F)			
10:05 - 10:30	Break			
10:30 - 12:35	ACS+DC 10 Analog and Data Converter Techniques (North Gate, B1F)	ETA 11 Technology and Circuit Techniques for IoT (South Gate, B1F)	MEM 12 Intelligent Memory System (West Gate, B1F)	DCS 13 Circuit Technologies for Security Enhancement (East Gate, B1F)
12:35 - 13:40	Lunch			
13:40 - 15:20	ACS 14 Inductive DC-DC Converters (North Gate, B1F)	DCS 15 Energy-Efficient Circuits and Architectures (South Gate, B1F)	WLN 16 Advanced Wireline Equalization (West Gate, B1F)	RF 17 Oscillators and Synthesizers (East Gate, B1F)
15:20 - 15:50	Break			
15:50 - 17:55	DC 18 (125) ADCs and Calibration Techniques (North Gate, B1F)	DCS+FPGA 19 (100) Multimedia and Signal Processing Hardware (South Gate, B1F)	SOC 20 (100) Intelligent Low-Power SoCs (West Gate, B1F)	RF 21 (100) Low-Power RF Transmitters and Receivers (East Gate, B1F)
17:55 - 19:30	Farewell Social Hour (Foyer, B1F)			

Day 1 November 5, 2018 (Monday)

[Tutorial 1]

TITLE	When SAR Meets $\Delta\Sigma$ - A Tale of Two ADC Architectures -
DATE / TIME	November 5, 2018 (Monday) / 9:00 AM - 10:30 AM
ROOM	South+West+East Gate, B1F
SPEAKER	Nan Sun, <i>University of Texas at Austin, USA</i>

Abstract:

SAR is widely used for medium resolution applications due to its simplicity, scaling compatibility, and low-power consumption. However, its power efficiency degrades as the resolution increases due to its tight requirement on the comparator noise and the exponentially growing capacitor DAC array. By contrast, $\Delta\Sigma$ ADC is a popular architecture for high-resolution applications. Taking advantage of noise shaping, it can achieve high resolution with a low-resolution quantizer and DAC. However, it typically requires the use of op-amps that are power hungry and scaling unfriendly.

This tutorial will review latest hybrid ADCs that aim to combine the merits of SAR and $\Delta\Sigma$ while simultaneously obviating their drawbacks. After presenting a high-level overview of published works, we will take a deep dive into two interesting noise-shaping SAR ADC architectures. The first one uses fully passive switched-capacitor filter to achieve 2nd-order noise shaping. It is fully dynamic and can be easily duty cycled. In addition, it is robust and calibration free. Thus, it is well suited for low-power sensor applications. The second one adopts an error-feedback structure, which simplifies the filter design. It consumes very low power by using a dynamic amplifier and address its process, voltage, and temperature (PVT) sensitivity via a fast-convergence background calibration loop.

Biography:

Nan Sun is Associate Professor at the University of Texas at Austin. He received the B.S. degree from Tsinghua University, China in 2006, where he ranked top in Department of Electronic Engineering. He received the Ph.D. degree from Harvard University in 2010. Dr. Sun received the NSF Career Award in 2013 and Jack Kilby Research Award from UT Austin in both 2015 and 2016. He won Harvard Teaching Award from 2008 to 2010. He serves in the TPC of IEEE Custom Integrated Circuits Conference and Asian Solid-State Circuit Conference. He is Associate Editor for IEEE Transactions on Circuits and Systems – I: Regular Papers, and Guest Editor for IEEE Journal of Solid-State Circuits. He is currently taking sabbatical at Tsinghua University until summer 2019.

[Tutorial 2]

TITLE	Wireless ECG Acquisition and Cardiac Stimulation SOC's for Body Sensor Networks
DATE / TIME	November 5, 2018 (Monday) / 10:50 AM - 12:20 AM
ROOM	South+West+East Gate, B1F
SPEAKER	Shuenn-Yuh Lee, <i>National Cheng Kung University, Taiwan</i>

Abstract:

There are several medical devices are made to monitor their heart to avert the heart diseases. Moreover, body sensor networks (BSNs) based applications or wearable devices have become more acceptable to the people for monitoring the real-time health information, such as the electrocardiogram (ECG). In order to enhance the portability of BSNs, a low-power wireless ECG acquisition system on a chip (SOC) stuck on the body is required. In this tutorial, a bio-signal acquisition system with the features of low power consumption, wireless transmission, and the on-time monitoring will be presented. Moreover, some researches have been reported that it is efficient to electrically generate neural action potential to control dysfunctional organs. Therefore, the telemetry integrated circuits will be required because they can provide coupling power and are able to transmit or receive data to or from according to implantable body sensor network. In this tutorial, a closed-loop implantable micro-stimulator system on chip (IMSoC), which possesses the sensing of a physiological signal, micro-stimulation, and wireless data/command transmission, will be also presented.

Biography:

Shuenn-Yuh Lee received the B.S. degree from the National Taiwan Ocean University, Keelung, Taiwan, in 1988, and the M.S. and Ph.D. degrees from the National Cheng Kung University, Tainan, Taiwan, in 1994 and 1999, respectively. He is currently a Professor at the Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan. From 2013 to 2016, he serves as the Chairman of IEEE Solid-State Circuits Society Tainan Chapter. From 2016 to 2017, he serves as the Vice Chairman of IEEE Tainan Section. He is the Associate Editor of IEEE Transaction on Biomedical Circuits and Systems from 2016-2019. His present research activities involve the design of analog and mixed-signal integrated circuits, biomedical circuits and systems, low-power and low-voltage analog circuits, and RF front-end integrated circuits for wireless communications.

[Tutorial 3]

TITLE	Terahertz CMOS Technology for Beyond 5G
DATE / TIME	November 5, 2018 (Monday) / 1:40 PM - 3:10 PM
ROOM	South+West+East Gate, B1F
SPEAKER	Minoru Fujishima, <i>Hiroshima University, Japan</i>

Abstract:

The fifth generation (5G) is about to begin in 2020. New applications are expected in 5G where data rate of 10 Gb/s and low delay of 1 ms are realized. Meanwhile, discussion on "Beyond 5G" after 10 years is beginning to start, since the mobile generation has evolved every decade.

The need for high-speed communication continues in the future since the data handled over the Internet is exponentially increasing. How can we realize the target communication speed of 100 Gb/s in Beyond 5G? One powerful candidate is a new communication technology using the 300-GHz band which is one of the terahertz bands. In this presentation, firstly, the evolution of communication speed is introduced, and the reason why wireless communication has dramatically increased the data rate will be discussed. Then, after the superiority of the 300-GHz band usable for wireless communication is introduced, CMOS technology for realizing the 300-GHz-band wireless communication is explained. Finally, how the world changes with beyond 5G using terahertz communication will be discussed.

Biography:

Minoru Fujishima received the B.E., M.E. and Ph.D degrees in Electronics Engineering from the University of Tokyo, Japan in 1988, 1990 and 1993, respectively. He joined faculty of the University of Tokyo in 1988 as a research associate, and was an associate professor of the School of Frontier Sciences, University of Tokyo since 1999. He was a visiting professor at the ESAT-MICAS laboratory, Katholieke Universiteit Leuven, Belgium, from 1998 to 2000. Since 2009, he has been a professor of the Graduate School of Advanced Sciences of Matter, Hiroshima University.

He studied design and modeling of CMOS and BiCMOS circuits, nonlinear circuits, single-electron circuits, and quantum-computing circuits. His current research interests are in the designs of low-power millimeter- and short-millimeter-wave wireless CMOS circuits. He coauthored more than 50 journal papers and 120 conference papers. He served as a distinguished lecturer in IEEE solid-state circuits society from 2011 to 2012.

[Tutorial 4]

TITLE	Memory System for Next Generation AI
DATE / TIME	November 5, 2018 (Monday) / 3:30 PM - 5:00 PM
ROOM	South+West+East Gate, B1F
SPEAKER	Kyomin Sohn, <i>Samsung Electronics, Korea</i>

Abstract:

Now, it is the era of deep learning and AI. Among various approaches to accelerate neural network calculation, HBM (high bandwidth memory) DRAM is one of key components in a state-of-the-art accelerators.

Basically, HBM DRAM shows unparalleled bandwidth like 1TB/s in a small SiP (system in package). To provide this huge bandwidth, there are many challenges like power density, thermal dissipation, testability and reliability from stacking and 2.5D configuration.

In this tutorial, the reasons for using HBM in accelerators are explained in detail, and the key schemes of HBM and difficulties of developing and using HBM will be discussed. Furthermore, the requirement of memory system for next generation AI and the promising features including near data processing are also touched.

Biography:

Kyomin Sohn received the B.S. and M.S. degrees in Electrical Engineering in 1994 and 1996, respectively, from Yonsei University, Seoul. From 1996 to 2003, he was with Samsung Electronics, Korea, involved in SRAM Design Team. He designed various kinds of high-speed SRAM devices.

He received the Ph.D. degree in EECS in 2007 from KAIST, Daejeon, Korea. He rejoined Samsung Electronics in 2007, where he has been involved in DRAM Design Team. He is a Master (Technical VP) in Samsung and he is responsible for development of HBM DRAM and Future Technology.

His interests include the next generation 3D-DRAM, robust memory design, and processing-in-memory for AI applications. Since 2012, he has currently served as a Technical Program Committee member of Symposium on VLSI Circuits.

[Student Design Contest] (SDC Exhibition)

DATE / TIME	November 5, 2018 (Monday) / 5:00 PM - 7:00 PM
VENUE	Foyer, B1F

[FPGA Demo]

DATE / TIME	November 5, 2018 (Monday) / 5:00 PM - 7:00 PM
VENUE	Foyer, B1F

Day 2 November 6, 2018 (Tuesday)

Opening Ceremony

DATE / TIME November 6, 2018 (Tuesday) / 8:30 AM - 08:50 AM
ROOM Far Eastern Grand Ballroom A+B, B2F

Session P 1: Plenary
Date / Time November 6, 2018 (Tuesday) / 8:50 AM - 10:25 AM
Room Far Eastern Grand Ballroom A+B, B2F
Chair Jae-Yoon Sim, POSTECH

[Plenary Talk 1]

TITLE Circuit Design in Nano-Scale CMOS Technologies
DATE / TIME November 6, 2018 (Tuesday) / 8:50 AM - 9:35 AM
SPEAKER Kevin Zhang, TSMC, Taiwan

Abstract:

The relentless pursuit of Moore's law by semiconductor industry has led the feature size of CMOS transistor well into nano-scale regime. Deeply scaled technologies have created many new challenges for circuit design, e.g., device variation and voltage head-room. In this presentation, an overview of today's semiconductor technology landscape will be presented first, including major innovations that have kept the scaling continue. Then the focus of this talk will be on how to address the scaling challenges with novel circuit design techniques, covering key circuit design areas, digital, memory, analog, and mixed signals. A number of real design examples will be used to illustrate the new design concepts that are proven to be effective in helping the scaling. A central theme throughout the presentation will be around the technology-design optimization in order to continue to harvest the benefits of technology scaling.

Keywords: Nano-Scale, CMOS

Biography:

Dr. Kevin Zhang currently serves as Vice President of Business Development. Prior to this role, Dr. Zhang served as Vice President of Design and Technology Platform. Before joining TSMC in November 2016, Dr. Zhang was Vice President of Technology and Manufacturing Group and Director of Circuit Technology at Intel, where he was responsible to the development of process design rules, circuit & device modeling, digital libraries, key analog and mixed-signal circuits. He led the development of embedded memory technologies from 90nm to 10nm at Intel. He was also responsible to the design and validation of lead vehicles for process technology development at Intel. Dr. Zhang was elected as Intel Fellow in 2005 and led his teams to win 5 Intel Achievement Awards, the highest technical accomplishments at the company.

Dr. Zhang has published more than 80 papers at international conferences and in technical journals and is the editor of Embedded Memory for Nano-Scale VLSIs, published by Springer in 2009. He holds 55 U.S. patents in the field of integrated circuit technology. Dr. Zhang was the 2016 International Solid-State Circuit Conference (ISSCC) Program chair and serves on IEEE VLSI Executive Committee. He is a Fellow of the Institute of Electrical and Electronics Engineers (IEEE). He received his bachelor's degree from Tsinghua University in Beijing and his Ph.D. from Duke University, both in electrical engineering.

[Plenary Talk 2]

TITLE

Open the New World of 5G

DATE / TIME

November 6, 2018 (Tuesday) / 9:40 AM - 10:25 AM

SPEAKER

Seizo Onoe, *NTT DOCOMO, DOCOMO Tech., Japan*

Abstract:

5G is stimulating people's imagination and expectations for a new world that it may bring about by the year 2020. 5G is aimed at meeting a wide range of requirements such as further enhanced mobile broadband, massive connections and reliable critical communications with low latency. Furthermore, it is highly expected to invent new business models and ecosystems across the industries.

In the presentation, first the history of mobile communications is reviewed to predict the future. Next, what 5G would create is discussed, which is followed by the discussion on 5G economics. Some concerns about the economics of 5G deployment are seen here and there because people tend to believe 5G would need a huge number of small cells due to limited coverage caused by higher spectrum bands. In the past, more than 30 years ago, no one believed the realization of the 2GHz cellular system. Mobile technologies have achieved many things that were once thought impossible, driven by semiconductor technology evolution. In the future, cost-effective 5G systems with millimeter waves must be realized by further evolved mobile and semiconductor technologies. Lastly, predictions are introduced being derived from the two laws that the speaker has defined. One is the law of previous generations' boom just before the next and the other is the law of great success only in even-numbered generations.

Keywords: 5G

Biography:

Seizo ONOE became Chief Technology Architect of NTT DOCOMO, INC in June 2017 after his 5 years tenure as Chief Technology Officer, while retaining the position of President of DOCOMO Technology, Inc. since June 2015. Prior to his current position, he was Chief Technology Officer and Executive Vice President and a Member of the Board of Directors of NTT DOCOMO from June 2012. Mr. Onoe became a Senior Vice President and Managing Director of the R&D Strategy Department in June 2008. He was a Vice President and took the position of Managing Director of departments in charge of Radio Access Network development from July 2002 to June 2008.

He has been responsible for leading initiatives in the research and development of the analog cellular system (1G), the digital cellular system (2G), W-CDMA/ HSPA (3G), LTE, LTE-Advanced (4G) and 5G. He has been working on the research and development of radio access networks, core networks, consumer devices and services. He has worked for NTT and NTT DOCOMO since 1982, acquiring more than 30 years of experience. Mr. Onoe has a master's degree in electronics from the Kyoto University Graduate School of Engineering.

Session	Industry 2: Advanced Techniques for Industrial Applications
Date / Time	November 6, 2018 (Tuesday) / 10:50 AM - 12:30 PM
Room	Far Eastern Grand Ballroom A+B, B2F
Chair	Daisaburo Takashima, Toshiba Memory Corp.
Co-Chair	Masaitsu Nakajima, Socionext

2-1

10:50 AM - 11:15 AM

A 12.4TOPS/W, 20% Less Gate Count Bidirectional Phase Domain Mac Circuit for DNN Inference Applications

Yosuke Toyama, Kentaro Yoshioka, Koichiro Ban, Akihide Sai, Kohei Onizuka
Toshiba Corporation, Japan

Abstract:

A small gate count 8 bit bidirectional phase domain MAC (PMAC) circuit is proposed for DNN inference engines. PMAC consumes significantly smaller power than standard fully digital MACs, owing to its efficient analog accumulation nature based on Gated-Ring-Oscillator (GRO). Compared with the previous first PoC of PMAC, the bidirectional architecture proposed in this paper achieves 20% less gate count, which is comparable with fully digital MACs, and relaxes system design constraints by eliminating phase error originating in leakage current. Asynchronous readout technique and 2-step DTC for the better system throughput and compact implementation, respectively, are presented for the first time. The PMAC achieves peak efficiency of 12.4 TOPS/W in 28 nm CMOS.

Keywords: DNN, MAC, Analog, GRO

2-2

11:15 AM - 11:40 AM

A Power and Area Efficient 2.5-16 Gbps Gen4 PCIe PHY in 10nm FinFET CMOS

Shenggao Li, Fulvio Spagna, Luke Tong, Sujatha Gowder, Rui Song, Ji Chen, Xiaoqing Wang, Wenyan Jia, Roan Nicholson, Michael De Vita, David Bradley, Matthew Duwe, Frank Verdico
Intel Corporation, United States

Abstract:

This paper presents a 2.5-16 Gbps Gen4 PCIe transceiver with 3-tap Tx EQ, and 8-tap Rx DFE in a 10nm FinFET CMOS technology. A low latency digital CDR is designed supporting a flexible timing recovery scheme. The CDR uses a 3-stage ring DCO, with a low-noise cascaded NMOS voltage regulator to provide 40dB PSRR with an operating temperature range from -40C to 125C. A senary-weighted hybrid C-DAC in the DCO achieves a monotonic fine tuning characteristic with a measured DNL of 0.3 LSB. The power efficiency is 7.5pJ/b, with a footprint of 129.6x945.0 um² per link.

Keywords: Gen4 PCIe, DCO, DFE, CTLE, CDR

2-3

11:40 AM - 12:05 PM

40-nm 64-kbit Buffer/Backup SRAM with 330 nW Standby Power at 65°C Using 3.3 V Io Moss for PMIC Less MCU in IoT Applications

Yoshisato Yokoyama, Tomohiro Miura, Yukari Ouchi, Daisuke Nakamura, Jiro Ishikawa, Shunya Nagata, Makoto Yabuuchi, Yuichiro Ishii, Koji Nii
Renesas Electronics, Japan

Abstract:

An effective standby power reduction of buffer/backup SRAM in MCU is proposed for power module IC (PMIC) less edge system in IoT applications. The proposed SRAM macro is implemented using 3.3 V thick gate-oxide IO MOSs for effectively reducing the leakage power with source bias control techniques. Four multiples interleave wordline circuitry is also introduced to reduce read and write operating power. A test chip with 64-kbit SRAM macro is designed and fabricated using 40-nm technology. The measured data show that the leakage power is 330 nW at 65°C, which is less 1/20 than other works. The read/write power is reduced by 40% by interleave wordline circuitry.

Keywords: Thick-gate transistor, SRAM, low leakage, standby power, dynamic power, retention

2-4**12:05 PM - 12:30 PM****Logic Process Compatible 40nm 256Kx144 Embedded RRAM with Low Voltage Current Limiter and Ambient Compensation Scheme to Improve the Read Window**

Chien-An Lai, Chung-Cheng Chou, Chi-Hsiang Weng, Zheng-Jun Lin, Pei-Ling Tseng, Chien-Fan Wang, Chih-Chen Wang, Tong-Chern Ong, Chi Chang, Yu-Der Chih, Tsung-Yung Chang

Taiwan Semiconductor Manufacturing Company, Taiwan

Abstract:

We present a low voltage current limiter that can effectively confine the filament size after forming or SET operations. The word-line (WL) location-aware and temperature compensation schemes are also proposed to deal with the ambient variations and tighten cell current distribution. Silicon data demonstrates a 9.5uA of read window can be achieved after 10KC retention test in 40nm logic process.

Keywords: RRAM, forming, compensation, read window

Session	ETA 3: Intelligent Sensor and Imager Systems
Date / Time	November 6, 2018 (Tuesday) / 10:50 AM - 12:30 PM
Room	East Gate, B1F
Chair	Shuenn-Yuh Lee, National Cheng-Kung University
Co-Chair	Shiro Doshio, Tokyo Institute of Technology

3-1

10:50 AM - 11:15 AM

A 10-Bit 1026-Channel Column Driver IC with Partially Segmented Piecewise Linear Digital-to-Analog Converters for Ultra-High-Definition TFT-LCDs with One Billion Color Display

Chih-Wen Lu¹, You-Gang Chang¹, Xing-Wei Huang¹, Jih-Siou Cheng², Po-Yu Tseng², Chih-Hsien Chou²

¹National Tsing Hua University, Taiwan; ²Novatek Microelectronics Corp., Taiwan

Abstract:

Herein, a 10-bit 1026-channel column driver IC with partially segmented piecewise linear digital-to-analog converters (DACs) is designed, simulated, and prototyped. This device is intended to improve the color depth and gamut of ultra-high-definition thin-film transistor liquid-crystal displays. The proposed column driver can output a precise gamma-corrected transfer curve without loss of effective bit resolution. An area-efficient two-voltage selector, a level shifter with a two-to-four decoder function, and a linearity-enhancing DAC-embedded operational amplifier are included in the design to minimize the overall chip area. The die dimensions of the 1026-channel column driver IC are only 18.14 mm × 1.2 mm. The prototype achieves a maximum settling time of 5.6 μ s for driving a load with 5-Kohm resistance and 300-pF capacitance within 10-mV tolerance of the final voltage.

Keywords: LCD column driver, DAC, ultra-HD, TFT-LCD, and DAC-embedded op-amp.

3-2

11:15 AM - 11:40 AM

A WDR CMOS Image Sensor Employing in-Pixel Capacitive Variation Using a Re-Configurable Source Follower for Low Light Applications

Neha Priyadarshini, Chandani Anand, Mukul Sarkar

Indian Institute of Technology, Delhi, India

Abstract:

A wide dynamic range image sensor that uses a 5-transistor pixel architecture to provide user-programmable conversion gain enhancement for detection of low illumination signals is presented. The dynamic range enhancement is a result of periodic variation of the gate-bulk capacitance of the in-pixel source follower by re-configuring it as a MOS capacitor. The pixel is capable of providing standard integrated photo-signal in high illumination and amplified signal in low illumination. A prototype sensor containing a 64 x 64 array of the proposed pixels has been fabricated in AMS 0.35 μ m, 3.3 V CMOS technology to verify the operation. The 10 μ m x 10 μ m pixel has a 20.25% fill factor. The in-pixel signal amplification results in a dynamic range enhancement of 18 dB under low illumination condition and a conversion gain enhancement of 160 μ V/e⁻.

Keywords: CMOS Image Sensor, Wide dynamic range, Low light imaging, Parametric Amplifier

3-3

11:40 AM - 12:05 PM

A CMOS Imager for Reflective Pulse Oximeter with Motion Artifact and Ambient Interference Rejections

Hsiang-Lin Chen, Tzu-Hsiang Hsu, Sung-En Hsieh, Chih-Cheng Hsieh

National Tsing Hua University, Taiwan

Abstract:

This paper presents a dual-mode CMOS imager for reflective pulse oximeter and fingerprint capturing capability. The same sensing array with 3-transistor active pixel sensor (3T-APS) is used in both modes for area and cost efficiency. In the oximeter mode, a coarse-fine ADC is applied to extend the system resolution. A periodical tracking and subtracting (PTS) technique is proposed to prevent the physiological signal (photoplethysmogram, PPG) from saturation caused by the motion artifact. The 60Hz time-varying ambient light from power line noise is suppressed by the post processing of the moving averaging filter with a sampling frequency (fs) of 120Hz. A prototype with 64×64-pixel array and 20×20μm² pixel pitch was fabricated in TSMC 0.18μm CMOS technology. The measured result shows a motion rejection capability of ±199× AC swing, a motion tracking speed of 61.4kHz, and an ambient interference rejection capability of -36dB. The achieved SpO₂ accuracy is ±0.51% (@SpO₂ = 97%) at a power consumption of 380μW (without LED driver).

Keywords: Ambient light rejection, Bio-signal sensors, Fingerprint sensor, Motion artifact rejection, Reflective pulse oximeter

3-4

12:05 PM - 12:30 PM

A 4-Channel, 5.04 μW, 0.325 mm², Parallel Neural Recording System Based on Orthogonal Sampling

Reza Ranjandish, Alexandre Schmid

EPFL, Switzerland

Abstract:

The application of orthogonal sampling for parallel neural recording is presented in this paper. Orthogonal sampling enables reducing the number of the ADCs in conventional recording systems into one single unit. Consequently, the ADC bandwidth and dynamic range is effectively employed and shared between all the channels without any loss in the temporal information of the channels during sampling, which is not the case of time-multiplexed ADCs. A 4-channel neural recording system based on orthogonal sampling is implemented in a 0.18 μm technology with a power consumption of 1.26 μW per channel supplied at 0.8 V to validate the proposed methodology.

Keywords: Neural recording, orthogonal sampling, capacitively-coupled instrumentation amplifier, neural activity

Session	ACS 4: Power Converters and Sensors
Date / Time	November 6, 2018 (Tuesday) / 1:30 PM - 3:10 PM
Room	North Gate, B1F
Chair	Po-Hung Chen, National Chiao Tung University
Co-Chair	Po-Chiun Huang, National Tsing Hua University

4-1

1:30 PM - 1:55 PM

An Integrated DC-DC Converter with Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery

U-Fat Chio¹, Kuo-Chih Wen¹, Sai-Weng Sin¹, Chi-Seng Lam¹, Yan Lu¹, Franco Maloberti², Rui Paulo Martins¹
¹University of Macau, Macau; ²University of Pavia, Italy

Abstract:

This paper presents a fully integrated VCO-based switched-capacitor (SC) DC-DC converter in 65 nm CMOS. We propose two transient-enhancement techniques: segmented frequency modulation (SFM) and multiphase co-work control (MCW). We design a 15-phase interleaved converter to support an output voltage of 1V from a 2.4V input supply, takes 29ns for output voltage recovering to steady state from load transients. It obtains a peak efficiency of 82.8 % and keeps the efficiency above 80 % from 31mA to 138mA. The SC DC-DC converter chip occupies 0.61mm², and its output power density is 240 mW/mm².

Keywords: SC DC-DC converter, fully integrated, switched-capacitor, voltage-controlled oscillator (VCO)

4-2

1:55 PM - 2:20 PM

An 88% Efficiency 2.4μW to 15.6μW Triboelectric Nanogenerator Energy Harvesting System Based on a Single-Comparator Control Algorithm

Karim Rawy¹, Ruchi Sharma¹, Hong-Joon Yoon², Usman Khan², Sang-Woo Kim², Tony Kim¹
¹Nanyang technological University in Singapore, Singapore; ²Sungkyunkwan University, Korea

Abstract:

This paper presents an energy harvesting system (EHS) based on a triboelectric nanogenerator (TENG). A novel TENG HDL spice model was developed to optimize the proposed ultra-low power (ULP) EHS. The proposed TENG-EHS utilizes a novel single-comparator-control (SCC) algorithm for improving the power conversion efficiency (PCE). It modulates the switching frequency of the implemented switched capacitor charge pump (SCCP) in proportion to the load condition at a given applied vibration frequency (i.e. excitation frequency). Moreover, a novel hysteresis control technique was introduced. It regulates the input voltage at the maximum possible power point without IC breakdown, and adopts a dropout excess charge storage technique. The fabricated test chip in 65-nm CMOS technology achieves a peak PCE of 88% with 2.4 μW to 15.6 μW input power and power density of 39.59 μW/mm².

Keywords: Energy Harvesting, Triboelectric Nanogenerator, Switched Capacitor Charge Pump, Power Management Circuit

4-3 (Short Paper)**2:20 PM - 2:32 PM****A Wide-Range Capacitive DC-DC Converter with 2D-MPPT for Soil/Solar Energy Extraction**I-Che Ou², Jia-Ping Yang², Chia-Hung Liu², Kai-Jie Huang², Kun-Ju Tsai¹, Yu Lee¹, Yuan-Hua Chu¹, Yu-Te Liao²¹Industrial Research and Technology Institute, Taiwan; ²National Chiao Tung University, Taiwan**Abstract:**

This paper presents a capacitive DC-DC converter with adaptive DC-DC conversion ratios and maximum power point tracking (MPPT) for soil and solar energy extraction. To overcome the varying input power ranges of the solar/soil energy sources, a two-dimension power tracking loop with time-based current slope detection was employed. The design was fabricated in a 0.18- μm CMOS process, achieving >80% efficiency in a throughput power range of 360 μW to 25mW in the soil mode and from 400 μW to 10mW in the solar mode while the peak system efficiency is 89.5%.

Keywords: DC-DC converter, energy harvesting, wide input range, CMOS

4-4 (Short Paper)**2:32 PM - 2:45 PM****A 13.56 MHz 88.7%-PCE Voltage Doubling Rectifier Using Adaptive Delay Time and Pulse-Width Control**Ye-Sing Luo², Hsing-Hung Lin¹, Shen-Iuan Liu¹¹National Taiwan University, Taiwan; ²Richtek Technology, Taiwan**Abstract:**

A voltage doubling rectifier using an adaptive pulse controller is presented to receive the low input amplitude. The adaptive pulse controller adjusts the delay time and pulse-width of the pulses in the background to control the power switches. By keeping the output voltage as high as possible, the power conversion efficiency (PCE) of this voltage doubling rectifier is enhanced. This work is fabricated in a 0.18 μm CMOS process. For the input amplitude of 0.8V, an input frequency of 13.56MHz, and a load resistor of 140 Ω , this rectifier achieves a PCE of 88.7%. For the input amplitude of 1.3V, the rectifier has a peak PCE of 89.3%

Keywords: voltage doubling, rectifier, adaptive delay time control, adaptive pulse-width control

4-5**2:45 PM - 3:10 PM****A 6800- μm^2 Resistor-Based Temperature Sensor in 180-nm CMOS**

Jan Angevare, Kofi Makinwa

Delft University of Technology, Netherlands

Abstract:

A resistor-based temperature sensor has been realized in 180 nm CMOS for SoC thermal management applications. Occupying only 6800 μm^2 , it is the smallest resistor-based temperature sensor ever reported. This is achieved by employing a compact highly-digital VCO-based ADC. After a 2-point trim, the sensor achieves an inaccuracy of $\pm 0.35^\circ\text{C}$ (3σ) in a temperature range from -35°C to 125°C . By achieving a resolution of 0.12°C (rms) at 2.8 kSa/s, it can track the fast thermal-transients in SoCs.

Keywords: Temperature Sensors, Thermal Sensing, Wien-Bridge

Session	FPGA 5: FPGA-based AI Computing
Date / Time	November 6, 2018 (Tuesday) / 1:30 PM - 3:10 PM
Room	South Gate, B1F
Chair	Tay-Jyi Lin, National Chung Cheng University
Co-Chair	Byungsub Kim, POSTECH

5-1

1:30 PM - 1:55 PM

FPGA-Based CNN Processor with Filter-Wise-Optimized Bit Precision

Asuka Maki, Daisuke Miyashita, Kengo Nakata, Fumihiko Tachibana, Tomoya Suzuki, Jun Deguchi
Toshiba Memory, Japan

Abstract:

Many efforts have been made to improve the efficiency for inference of deep convolutional neural network. To achieve further improvement of the efficiency without penalty of accuracy, we propose filter-wise optimized quantization with variable precision and the hardware architecture that fully supports it, i.e. as the bit precision for operations is reduced by granularly optimizing weight bit precision filter-by-filter, the execution time is reduced proportionally to the total number of computations multiplied with the number of weight bit. We implement the proposed architecture on FPGA and demonstrate that ResNet-50 run with 5.3x less execution cycles without penalty of accuracy.

Keywords: Deep Learning, Convolutional Neural Network, Quantization, Variable Bit Width, FPGA

5-2

1:55 PM - 2:20 PM

An Asynchronous Energy-Efficient CNN Accelerator with Reconfigurable Architecture

Weijia Chen², Hui Wu², Shaojun Wei², Anping He¹, Hong Chen²
¹Lanzhou University, China; ²Tsinghua University, China

Abstract:

We introduce a very high energy-efficient convolutional neural network (CNN) accelerator with an asynchronous and reconfigurable architecture. With a dynamically reconfigurable architecture, the data path, calculation method, the activation function, pooling way and size can be changed. The global clock is replaced by the local pulse signals from Click elements. And an asynchronous pipeline formed by Click elements in series to ensure the speed. The input data reuse and the integration computing pattern an 88% decrease of the access to off-chip memory. The LeNet-5 is verified with the FPGA of Xilinx VC707. The asynchronous computing core has 84% less dynamic power than the synchronous core and The accelerator's efficiency achieves 30.03 GOPS/W, 2.1 times better than the best result of previous works.

Keywords: CNN accelerator, Asynchronous circuit, Energy-Efficient

5-3

2:20 PM - 2:45 PM

Hardware Architecture for Fast General Object Detection Using Aggregated Channel Features

Koichi Mitsunari, Jaehoon Yu, Masanori Hashimoto

Osaka University, Japan

Abstract:

High detection accuracy and fast detection must be achieved within a limited power budget for embedded system applications. This paper proposes an embedded system-oriented hardware accelerator for object detection with aggregated channel features (ACF). The proposed accelerator consists of hardware architectures dedicated for HOG features, quantization, and boosted decision trees, and they contribute to 2006X speed-up and 601X memory reduction. Our FPGA implementation result shows that the proposed accelerator can detect pedestrians in 170 fps for Full HD images, and 6-class traffic objects in 78 fps for Full HD images.

Keywords: Object Detection, Hardware Accelerator, Aggregated Channel Features

5-4

2:45 PM - 3:10 PM

A Neural Network Accelerator with Integrated Feature Extraction Processor for a Freezing of Gait Detection System

Val Mikos², Chun-Huat Heng², Arthur Tay², Shih-Cheng Yen², Nicole Shuang Yu Chia¹, Karen Mui Ling Koh¹, Dawn May Leng Tan³, Wing Lok Au¹

¹*National Neuroscience Institute, Singapore;* ²*National University of Singapore, Singapore;* ³*Singapore General Hospital, Singapore*

Abstract:

Parkinson's disease patients are at risk of falls due to freezing of gait (FoG). Wearable detection systems providing biofeedback for aid rely on accurate FoG classifiers, but such algorithms have yet to propose a dedicated hardware implementation. This paper is a first proposal of a dedicated hardware for a real-time FoG feature extractor and classifier on a single chip. The design exploits an FoG system's inherent time-sharing affinity to reduce area consumption. When mapped onto an FPGA, the design surpasses previous FoG detection system hardware in terms of wearability, power efficiency and classification accuracy.

Keywords: FPGA, System on chip, Wearable electronics, Machine learning, Parkinson's disease, Freezing of Gait

Session	WLN 6: Optical Link and CDR
Date / Time	November 6, 2018 (Tuesday) / 1:30 PM - 3:10 PM
Room	West Gate, B1F
Chair	Ching-Yuan Yang, National Chung-Hsing University
Co-Chair	Jun Terada, NTT

6-1

1:30 PM - 1:55 PM

A 0.25-27Gb/S Wideband PAM4/NRZ Transceiver with Adaptive Power CDR for 8K System

Yoshihide Komatsu, Akinori Shinmyo, Masami Funabashi, Shuji Kato, Kazuya Hatooka, Kenji Tanaka, Mayuko Fujita, Kouichi Fukuda
Panasonic, Japan

Abstract:

A multimodal PAM4/NRZ transceiver, including adaptive ultra-wide range receiver and power noise stabilized transmitter, is proposed. An adaptive CDR controller selects the optimum CDR mode according to transmitter jitter performance to reduce power consumption while ensuring interoperability. The multimodal transmitter features PAM4 emphasis driver and stabilizer, which are applied for reducing distortion impact and power induced jitter. A test chip was fabricated in 28nm CMOS process and achieved 0.25-27Gb/s wide-range operation, and it achieves 33% power reduction compared to conventional architecture without the adaptive controller, resulting in 3.8pJ/bit energy efficiency for TX and 6.2pJ/bit for RX.

Keywords: Wireline, Transceiver, PAM4, CDR

6-2

1:55 PM - 2:20 PM

A Fully-Integrated 25Gb/S Low-Noise TIA+CDR Optical Receiver Designed in 40nm-CMOS

Juncheng Wang², Xuefeng Chen³, Shang Hu², Yaxin Cai³, Rui Bai³, Xin Wang³, Yuanxi Zhang³, Shenglong Zhuo³, Bozhi Yin², Chang Liu², Milton Lu³, Nan Qi¹, Patrickyin Chiang²

¹Chinese Academy of Sciences, China; ²Fudan University, China; ³PhotonIC Technology, China

Abstract:

A fully-integrated 25Gbps low-noise optical receiver is presented that integrates a Transimpedance Amplifier (TIA), Continuous-Time Linear Equalizer (CTLE), high gain and high bandwidth Limiting Amplifier (LA), and Clock and Data-Recovery (CDR) into a single die. The TIA employs an inverter-based pseudo differential TIA with Cross-Coupled Negative Gm pair and a Negative capacitor to increase the signal bandwidth, while a MOSFET Corner Compensation (MCC) circuit compensates for the CMOS corner variation. An Automatic Gain Control (AGC) scheme is proposed that solves the group delay issue caused by TIA input impedance variation from small input to overload current. Finally, a 2x-oversampling CDR using a bang-bang phase detector is included. The 850nm VCSEL-based full-link measurement results show that the optical receiver achieves a sensitivity (BER<1e-12) of 52uApp (RSSI Current, ER=4.89dB) with a 150ff Photodiode from the 3.3V and 1.2V supplies, respectively.

Keywords: low noise, optical receiver, corner compensation, auto gain control, CDR

6-3

2:20 PM - 2:45 PM

A Low Input Referred Noise and Low Crosstalk Noise 25 Gb/S Transimpedance Amplifier with Inductor-Less Bandwidth Compensation

Akitaka Hiratsuka¹, Akira Tsuchiya³, Kenji Tanaka², Hiroyuki Fukuyama², Naoki Miura², Hideyuki Nosaka², Hidetoshi Onodera¹

¹Kyoto University, Japan; ²NTT, Japan; ³The University of Shiga Prefecture, Japan

Abstract:

This paper presents a low-noise and high-speed transimpedance amplifier (TIA) for optical interconnection. For high density parallel integration of optical receiver, small area and crosstalk mitigation are important as well as high speed, low power and so on. We propose an inverter TIA (INV-TIA) with inductor-less bandwidth compensation circuits and a passive crosstalk filter. Since these additional circuits are composed with resistance and capacitance, the area overhead and the power overhead are much smaller than existing techniques. We fabricated 25 Gb/s TIA in a 65-nm CMOS. Compared to the reference design, the proposed circuit reduces the input referred noise by 60% and the crosstalk noise by 25%.

Keywords: Transimpedance amplifier, optical communication

6-4

2:45 PM - 3:10 PM

A 10-Gb/S, 0.03-mm², 1.28-pJ/Bit Half-Rate All-Digital Injection-Locked Clock and Data Recovery with Maximum Timing-Margin Tracking Loop

Min-Seong Choo, Han-Gon Ko, Sung-Yong Cho, Kwangho Lee, Deog-Kyoon Jeong
Seoul National University, Korea

Abstract:

A 10-Gb/s, 0.03-mm², 1.28-pJ/bit half-rate all-digital injection-locked clock and data recovery (ILCDR) with a path mismatch tracking (PMT) loop is presented. When injection timing is not perfectly matched with the local oscillator, the timing margin of the data sampler is reduced, resulting in the degradation of jitter tolerance (JTOL) performance. By simply de-serializing the error information from the phase detector in the conventional phase-locked loop (PLL) based CDR with respect to the polarity of the data transition, the proposed ILCDR achieves robust injection behavior over path mismatch variations. Fabricated in 28-nm CMOS technology, the proposed ILCDR occupies 0.03 mm² and consumes 12.8 mW at 10 Gb/s with a 0.9-V supply voltage. The measured JTOL is 1 UI_{pp} at 31 MHz with the target bit error rate of 10⁻¹² in the presence of the initial path delay mismatch.

Keywords: clock and data recovery, injection-locked oscillator, injection-locked CDR, path mismatch tracking, jitter tolerance, half rate

Session	RF 7: Millimeter-Wave Transceivers and Terahertz Sensors
Date / Time	November 6, 2018 (Tuesday) / 1:30 PM - 3:10 PM
Room	East Gate, B1F
Chair	Minoru Fujishima, Hiroshima University
Co-Chair	Tae Wook Kim, Yonsei University

7-1

1:30 PM - 1:55 PM

A 28.16-Gb/s Area-Efficient 60GHz CMOS Bi-Directional Transceiver for IEEE 802.11ay

Jian Pang, Korkut Tokgoz, Shotaro Maki, Zheng Li, Xueting Luo, Ibrahim Abdo, Seitarou Kawai, Hanli Liu, Bangan Liu, Makihiko Katsuragi, Kento Kimura, Atsushi Shirane, Kenichi Okada
Tokyo Institute of Technology, Japan

Abstract:

This paper introduces a 60-GHz CMOS transceiver designed for IEEE 802.11ad/ay featuring the area-efficient bi-directional operation. The proposed bi-directional PA-LNA occupies for less than half on-chip area, while staying a similar performance with the conventional standalone PA and LNA. The measured noise figure in RX mode is 4.8dB at 62.56GHz and the measured EVM is -26dB in TX mode with an output power of -4.2dBm. Thanks to the compact PA-LNA, this work realizes a maximum data-rate of 28.16Gb/s in 16QAM with only 3 square mm. The power consumption is 105mW in TX mode and 128mW in RX mode.

Keywords: 60 GHz, CMOS, transceiver, bi-directional, four-channel bonding

7-2

1:55 PM - 2:20 PM

A 77-GHz Mixed-Mode FMCW Generator Based on a Vernier TDC with Dual Rising-Edge Fractional-Phase Detector

Jianxi Wu¹, Zipeng Chen¹, Wei Zheng³, Yibo Liu¹, Shufu Wang³, Nan Qi², Baoyong Chi¹

¹*Institute of Microelectronics, Tsinghua University, China;* ²*Institute of Semiconductors, Chinese Academy of Sciences, China;* ³*Radarchip Technology Co., Ltd., China*

Abstract:

A 77-GHz mixed-mode FMCW generator is presented in this paper. A dual rising-edge fractional-phase detector and a 2.3 ns detection range, 10 ps resolution Vernier TDC with automatic calibration are proposed to overcome the issue caused the rising and falling time mismatch. A coarse-fine segmented DAC and a divider-less frequency error estimator are employed to reduce area. A sampling edge selection technique is utilized to remove glitches. An LC VCO with split varactors is proposed. The presented FMCW generator is implemented in 65nm CMOS and less than 251 kHz RMS frequency error is achieved.

Keywords: Frequency-modulated continuous-wave (FMCW), radar, mm-wave, PLL, Vernier TDC, Glitch, Segmented DAC

7-3

2:20 PM - 2:45 PM

A CMOS 76-81 GHz 2TX 3RX FMCW Radar Transceiver Based on Mixed-Mode PLL Chirp Generator

Taikun Ma¹, Zipeng Chen¹, Jianxi Wu¹, Wei Zheng³, Shufu Wang³, Nan Qi², Baoyong Chi¹

¹*Institute of Microelectronics, Tsinghua University, China;* ²*Institute of Semiconductors, Chinese Academy of Sciences, China;* ³*Radarchip Technology Co., Ltd., China*

Abstract:

A fully integrated 76-81 GHz frequency-modulated continuous-wave (FMCW) radar transceiver (TRX) in 65nm CMOS is presented. Two transmitters (TXs) and three receivers (RXs) are integrated for MIMO processing. A 38.5 GHz mixed-mode PLL with reconfigurable loop bandwidth and frequency doubling scheme are employed to generate the reconfigurable FMCW chirp waveforms. Passive voltage-mode down-conversion is utilized to improve the RX linearity against TX leakage. A bottom-switching PA is proposed to realize the Bi-Phase modulation, and the magnetically-coupled resonator technique is widely used to effectively expand the link bandwidth.

Keywords: Radar, frequency-modulated continuous-wave (FMCW). mm-wave, transceiver, PLL, CMOS

7-4

2:45 PM - 3:10 PM

A 25 fps 32×24 Digital CMOS Terahertz Image Sensor

Tong Fang, Run-Jiang Dou, Li-Yuan Liu, Jian Liu, Nan-Jian Wu

Institute of Semiconductors, Chinese Academy of Sciences, China

Abstract:

A 32×24 digital CMOS terahertz image sensor for 25 fps imaging at 860 GHz is presented. Pixel with DRC free structure is proposed and column parallel readout architecture is employed. The sensor array and the readout circuits are fully integrated into one single silicon chip in 180 nm CMOS process. Measured averaged room-temperature responsivity of single pixel is 1.28 kV/W at 860 GHz. The THz image sensor can operate up to 25 fps under continuous-wave illumination, and we acquired a video of a rotating blade chopping the backward wave oscillator (BWO) source beam, and the rotating blade can be clearly distinguished in the video.

Keywords: Terahertz imaging, CMOS Terahertz image sensor, DRC free patch antenna, Column parallel readout

Session	PD 8: Panel Discussion
Date / Time	November 6, 2018 (Tuesday) / 3:30 PM - 5:30 PM
Room	Far Eastern Grand Ballroom B, B2F
Moderator	Meng-Fan (Marvin) Chang, National Tsing Hua University

8-1

3:30 PM - 5:30 PM

The circuits and systems for Mobile AI

Abstract:

Recently, many new technology, circuits and systems are proposed to realize AI on silicon. Analog circuits look promising for design of the neuromorphic chips but digital implementations are still the main stream technology. Moreover, PiM with non-volatile memory is researched as the next technology for the AI realization. Especially, for the mobile AI intelligence, we need ultra-low power circuits and systems.

- Do you think Digital AI solutions will win over analog? Why?
- FPGA is enough rather than ASIC for the AI system?
- Do you prefer Analog circuits and systems for AI chip?
- What kind of low power/low energy schemes will be required?
- What kind of security schemes will be required for AI chip?
- Which type of memories are good to realize AI solutions?
- Will PiM be the mainstream AI system?
- Will circuit level innovation win over software innovation in AI?

Organizer: Tsung-Hsien Lin (National Taiwan University)

Co-organizer: Zhihua Wang (Tsinghua University)

Moderator: Meng-Fan (Marvin) Chang (National Tsing Hua University)

Panel Overview (+ brief AI trend): Meng-Fan (Marvin) Chang (National Tsing Hua University)

Panelists / Position:

- 1. Digital will win:** Robert Chen-Hao Chang (National Chung Hsing University)
- 2. Where can be Analog the MUST:** Jae-Yoon Sim (POSTECH)
- 3. Intelligent storage for AI:** Ken Takeuchi (Chuo University)
- 4. Compute location:** Shigeki Tomishima (Intel Corporation)
- 5. Memory Hierarchy in AI:** Kyomin Sohn (Samsung Electronics)
- 6. AI Architecture (FPGA vs. ASIC or Reconfigurable):** Masato Motomura (Hokkaido University)
- 7. AI Security:** Massimo Alioto (National University of Singapore)

Day 3 November 7, 2018 (Wednesday)

Session	P 9: Plenary
Date / Time	November 7, 2018 (Wednesday) / 8:30 AM - 10:05 AM
Room	Far Eastern Grand Ballroom A+B, B2F
Chair	Mototsugu Hamada, Keio University

[Plenary Talk 3]

TITLE	Practical Challenges in Supporting Functions in Memory
DATE / TIME	November 7, 2018 (Wednesday) / 8:30 AM - 9:15 AM
SPEAKER	Nam Sung Kim, <i>Samsung, Korea</i>

Abstract:

As data transfers between processors and memory become the performance and energy-efficiency bottleneck, supporting Functions in Memory (FIM) has emerged as an attractive computing paradigm. This plenary talk covers various challenges in making FIM practical especially for industry adoption. Specifically, it will first give insight on why it is hard to offer higher bandwidth and lower latency for processors/accelerators in memory unlike most researchers assume. Second, it will describe various technical challenges to make FIM synergistically work with existing computers. Lastly, it will discuss future directions for the research community to make FIM more practical.

Keywords: Memory, Supporting Functions

Biography:

Dr. Nam Sung Kim has worked on interdisciplinary research topics incorporating device, circuit, architecture, and system software for energy-efficient computing systems. Before he joined Samsung as a Sr. VP, he was a tenured faculty member of the University of Illinois, Urbana-Champaign and the University of Wisconsin, Madison. He received BS and Ph.D. degrees from KAIST and the University of Michigan, Ann Arbor, respectively. He has published more than 180 refereed articles to highly-selective conferences and journals in the field of digital circuit, processor architecture, and computer-aided design. The top three most frequently cited papers have more than 3500 citations and the total number of citations of all his papers exceeds 8400. He was a recipient of the ACM/IEEE International Symposium on Microarchitecture (MICRO) Best Paper Award, ACM/IEEE Most Influential International Symposium on Computer Architecture (ISCA) Paper Award, IEEE Micro Top Picks. He is a member of IEEE International Symposium on High-Performance Computer Architecture (HPCA) Hall of Fame and MICRO Hall of Fame.

[Plenary Talk 4]**TITLE****AI Drive Domain Specific Processor****DATE / TIME****November 7, 2018 (Wednesday) / 9:20 AM - 10:05 AM****SPEAKER****Yi Kang, UNISOC, China*****Abstract:***

Today most of hardware solutions for Artificial Intelligence (AI) use one of the following approaches, general purpose CPU GPU, or ASIC. While CPU and ASIC represent two extremes in term of efficiency and flexibility, GPU is more widely used and is a good compromise of different approaches. Domain Specific Processor or Domain Processor was proposed in recent years to meet with challenge of AI. Actually GPU can be considered as an example of Domain Processor, it is a PE mesh that is good for pixel based operations which consists of multiply, add that can be carried out in a massive parallel way. As AI evolves very dynamically and fast in recent year and perceivably in future, it calls for new type of Domain Processors. Currently most of AI hardware solutions are aiming at speeding up computations in Convolution Neural Network (CNN) where more than 80% of its computation is consisted of a series of dot products. ASIC type of solutions are efficient at performing parallel multiply-accumulate (MAC) operations in CNN but they are not fit for other type operations. There are other types of operations in CNN, for example, floating point division, permutations, operations for pruning sparse matrix etc. According to Amdahl Law, these operations need to be speed up otherwise total speedup is limited. Moreover, more and more new AI algorithms are developed in which percentage of MAC operations is less dominant compared to CNN. In this talk it is described that Domain Processor will be a trend in AI hardware development . The reason is that Domain Processor can provide enough horse power to meet AI's hunger for computation while provide good flexibility and programming ability at the same time for AI's evolution along its course. Compared to general purpose CPU, Domain Processor has better power consumption and better performance; Compared to ASIC, Domain Processor is more flexible and is equivalent in performance. In the talk Vector Processing is presented as an important feature for AI Domain Processor. Vector Processing is good at computation intensive load such as sparse matrix operations, permutations, general type of floating point operations and Vector Processor usually can provide enough memory bandwidth to support large number of computations, thus Vector Processor is good for AI applications. Recent development for AI on general purpose CPU architecture such as ARM suggests this point too. Some of important features for AI Domain Processor are also mentioned in the talk.

Keywords: AI, Domain Specific Processor

Biography:

Dr. Yi Kang is currently Chief Scientist and Senior Vice President at UNISOC (formally known as Spreadtrum), in charge of research and development for advanced technologies including 5G, AI and CPU. He joined in Spreadtrum in 2003 and was the overall project leader for many key IC development projects including the industry's first TD-SCDMA baseband chip, China's first mobile CPU core, company's first 4G multimode baseband chip and first mobile TV chip etc. Before joining Spreadtrum, Dr. Kang has more than 10 years engineering development and management experience with a few high-tech companies in field of high performance microprocessor, DSP, network security in US.

Dr. Yi Kang has published 14 papers in journals and conferences, he has 40 US and China patents as co-inventor. His current research interest is in wireless communication, microprocessor architecture and high speed digital circuit implementation. He is a member of China IMT-2020 Working Group that is a major 5G Alliance in China with experts from industry, universities and government agencies, he is also a director

of China Communication Standardization Association. Dr. Yi Kang received his BE and ME both from Tsinghua University in Beijing in Electronic Engineering, and PhD from University of Illinois at Urbana-Champaign in Computer Science.

Session	ACS+DC 10: Analog and Data Converter Techniques
Date / Time	November 7, 2018 (Wednesday) / 10:30 AM - 12:35 PM
Room	North Gate, B1F
Chair	Sai-Weng Sin, University of Macau
Co-Chair	Tsung-Heng Tsai, National Chung Cheng University

10-1

10:30 AM - 10:55 AM

A 3.9uW, 81.3dB SNDR, DC-Coupled, Time-Based Neural Recording IC with Degeneration R-DAC for Bidirectional Neural Interface in 180nm CMOS

Hyuntak Jeon², Jun-Suk Bang³, Yoontae Jung², Taeju Lee², Yeseul Jeon², Seok-Tae Koh², Jaesuk Choi², Doojin Jang², Soonyoung Hong¹, Minkyu Je²

¹Daegu Gyeongbuk institute of Science and Technology, Korea; ²Korea Advanced Institute of Science and Technology, Korea; ³Samsung Electronics, Korea

Abstract:

This paper presents a 5-bit VCO-based neural recording IC, which directly quantizes the input signal and achieves a large dynamic range (DR) to process the small-amplitude neural signal in the presence of the large-amplitude stimulation artifact (SA). A feedback-controlled source degeneration is applied to the input transistor circuit ($G_{m,in}$) by using a resistor DAC (R-DAC). It mitigates the circuit nonlinearity, resulting in a large signal-to-noise-and-distortion ratio (SNDR) and a high input impedance (Z_{in}). The implemented neural recording IC achieves 81.3dB SNDR over 200Hz signal bandwidth and 200mVpp maximum allowable input range while consuming 3.9uW per channel.

Keywords: Bidirectional Neural Interface, Resistor DAC, Delta-Sigma Modulator

10-2

10:55 AM - 11:20 AM

A Second-Order Purely VCO-Based CT $\Delta\Sigma$ ADC Using a Modified DPLL in 40-nm CMOS

Yi Zhong⁴, Shaolan Li³, Arindam Sanyal², Xiyuan Tang³, Linxiao Shen³, Siliang Wu¹, Nan Sun³

¹Beijing Institute of Tech., China; ²The State University of New York at Buffalo, Buffalo, United States;

³University of Texas, Austin, United States; ⁴University of Texas, Austin. Beijing Institute of Tech., United States

Abstract:

This paper presents a power-efficient purely VCO-based 2nd-order CT $\Delta\Sigma$ ADC featuring a modified DPLL structure. It combines a VCO with an SRO-based TDC, which enables 2nd-order noise shaping without any OTA. The nonlinearity of the front-end VCO is mitigated by putting it inside a closed loop. A multi-PFD scheme reduces the VCO center frequency and power. The proposed architecture also realizes an intrinsic tri-level DWA. A prototype ADC in 40-nm CMOS process achieves a Schreier FoM of 170.3 dB with a DR of 72.7 dB over 5.2-MHz BW, while consuming 0.91 mW under 1.1-V supply.

Keywords: time domain signal processing, VCO-based delta sigma ADC, DPLL, SRO, TDC, DWA

10-3 (Short Paper)**11:20 AM - 11:32 AM****An 11b 1GS/S Time-Interleaved ADC with Linearity Enhanced T/H**

Yan Zhu, Chi Hang Chan, Rui Martins

*University of Macau, China; University of Macau, Portugal; University of Macau, Macau***Abstract:**

This paper presents a 1GS/s 11 bit $4 \times$ Time-Interleaved (TI) ADC employing the proposed Track-and-Hold (T/H) to enhance the sampling linearity and avoid timing skews. A dual auxiliary Source-Follower (SF) T/H provides signal double boosting to suppress the sampling distortion while maintaining good power efficiency. We present a dynamic SF-based switch boosting technique, providing a fast signal boost up and less signal attenuation to maximize the tracking duration and V_{gs} of the sampling switch. A prototype in 65nm CMOS achieves SNDR of 55.8dB @Nyquist input and ERBW up to $2 \times$ Nyquist input with total 22mW power.

Keywords: Sampling front-end, Time-interleaved ADC, Pipelined SAR ADC, Offset calibration

10-4 (Short Paper)**11:32 AM - 11:45 AM****A 1-V 3.1-Ppm/°C 0.8-μW Bandgap Reference with Piecewise Exponential Curvature Compensation**

Hongrui Luo, Quan Sun, Ruizhi Zhang, Hong Zhang

*School of Electronic and Information Engineering, Xi'an Jiaotong University, China***Abstract:**

This paper presents a low-power precision BGR, which is realized with a current-mode BGR compensated by a piecewise exponential current generated by three simple differential MOS pairs. Fabricated in a 0.18-μm CMOS process, measured results show that the BGR achieves average and best TCs of 7.08 and 3.1 ppm/°C, respectively, in the range of -40 to 125°C, and a line sensitivity of 0.03% in a supply voltage range from 1 to 3V. The current consumption is 0.8 μA under a 1-V supply.

Keywords: Bandgap Reference

10-5**11:45 AM - 12:10 PM****A 40nW, Sub-1V Truly 'digital' Reverse Bandgap Reference Using Bulk-Diodes in 16nm FinFet**

Matthias Eberlein, Georgios Panagopoulos

*Intel Germany, Germany***Abstract:**

We present a novel, simple concept to generate a robust voltage reference, which is based on capacitive bias of pn-junctions. The respective PTAT and CTAT signals are sampled from the voltage-decay by means of different timings, and combined through charge sharing. This provides for precise current ratios of $N > 10000$, resulting in exceptionally large PTAT and reverse-bandgap levels. - Here, for the first time, the Nwell/Psub diode of a standard CMOS process is utilized in replacement of parasitic BJTs. The measured samples, on $2200\mu\text{m}^2$ active area in 16nm FinFet, achieve an untrimmed accuracy of $\pm 0.82\%$ (3σ) at 235mV output. Line sensitivity is 0.7mV/100mV, operating at a minimum supply of 0.85V with 47nA power drain. The compact Bandgap circuit is "digital" to that effect that no amplifiers, resistors, biasing or matching currents are required, neither is it impacted by any analog transistor performance.

Keywords: Bandgap voltage reference, FinFet process, bulk-diode, switched-capacitor

10-6

12:10 PM - 12:35 PM

A 0.6V 1.63fJ/c.-S. Detective Open-Loop Dynamic System Buffer for SAR ADC in Zero Capacitor TDDI System

Yao-Sheng Hu, Li-Yu Huang, Hsin-Shu Chen
National Taiwan University, Taiwan

Abstract:

A low-power detective open-loop dynamic (DeOLD) system buffer for SAR ADC without external-decoupling capacitor is proposed. It is suitable for the zero capacitor touch with display driver integration (TDDI) system. This system buffer actively predicts the input signal to quickly supplement the charge loss back. The dynamic charge sharing technique reduces 42.4% chargers power than that of the pump squeezing technique. Without external-decoupling capacitor, this detective open-loop dynamic system buffer with a 400kS/s 10b SAR ADC consumes 334nW under a 0.6V supply. Its active area only occupies 0.0098mm². It achieves 55.96dB of SNDR, which results in an FoMW of 1.63fJ/c.-s.

Keywords: SAR ADC, open-loop, dynamic operation, power system and zero capacitor TDDI technology

Session	ETA 11: Technology and Circuit Techniques for IoT
Date / Time	November 7, 2018 (Wednesday) / 10:30 AM - 12:35 PM
Room	South Gate, B1F
Chair	Minkyu Je, KAIST
Co-Chair	Ping-Hsuan Hsieh, National Tsing Hua University

11-1

10:30 AM - 10:55 AM

Design of a 2.45-GHz RF Energy Harvester for SWIPT IoT Smart Sensors

Pengcheng Xu, Denis Flandre, David Bol

Université catholique de Louvain, Belgium

Abstract:

In this paper, we study the design of a 2.45-GHz RF energy harvester system for SWIPT IoT application. For 2.45-GHz operation, we propose a parasitic-aware sizing of pi matching network. MPPT is used to help reaching target matched impedance at given input RF power. Measurement results show sensitivity as low as -16.5dBm with a peak power harvesting efficiency of 48.3% at -3dBm 2.45-GHz input RF power. Comparison between simulation and measurement results demonstrate that these results are limited by the parasitic capacitance and that PHE around 45% can be obtained down to -10dBm with PCB/package improvement for lower parasitic capacitance.

Keywords: RF energy harvester, 2.45-GHz, maximum power point tracking, power harvesting efficiency, impedance matching

11-2

10:55 AM - 11:20 AM

A 6.78-200 MHz Offset-Compensated Active Rectifier with Dynamic Logic Comparator for mm-Size Wirelessly Powered Implants

Jianming Zhao, Yuan Gao

Institute of Microelectronics, ASTAR, Singapore, Singapore

Abstract:

this paper presents an active rectifier with scalable operation frequency from 6.78MHz to 200MHz for mm-size wireless powered implantable medical device. A dynamic logic comparator with no static power consumption is proposed to work up to 200MHz. To compensate the intrinsic delay of comparator, a sample and hold (S/H) offset compensation loop is proposed. Implemented in a 65nm CMOS process, measurement results show that the rectifier achieves 95% voltage conversion ratio, 94% peak power conversion efficiency at 6.78MHz and 83% voltage conversion ratio, 84% peak efficiency at 200MHz.

Keywords: active rectifier, mm-size implants

11-3

11:20 AM - 11:45 AM

Photovoltaic-Assisted Self-V_{th}-Cancellation CMOS RF Rectifier for Wide Power Range Operation

Ren Usami, Takao Komiyama, Yasunori Chonan, Hiroyuki Yamaguchi, Koji Kotani

Akita Prefectural University, Japan

Abstract:

A photovoltaic (PV)-assisted self-V_{th}-cancellation (SVC) CMOS RF rectifier circuit for energy harvesting from ambient radio waves has been developed. Since the threshold voltage (V_{th}) of MOSFETs in the rectifier was effectively compensated for by a DC bias voltage generated from not only on-chip PV cells but also output voltage of the rectifier circuit itself, the PCE under low input power conditions was improved. In addition, a bias voltage limiting mechanism was newly adopted to appropriately suppress the excess bias voltage for threshold voltage compensation and to improve the PCE under high input power conditions. As a result, the rectifier circuit operates with higher efficiency than previously reported rectifiers over a wide input power range from as low as -25 dBm to higher input power without degradation in PCE.

Keywords: energy harvesting, photovoltaic, radio waves, rectifier

11-4

11:45 AM - 12:10 PM

Stable, Self-Biased and High-Gain Organic Amplifiers with Reduced Parameter Variation Effect

Masoud Seifaei¹, Daniel De Dorigo¹, David Ingvar Fleig¹, Matthias Kuhl¹, Ute Zschieschang², Hagen Klauk², Yiannos Manoli¹

¹Albert Ludwigs University of Freiburg, Germany; ²Max Plank Institute for Solid State Research, Germany

Abstract:

This paper presents the design and implementation of self-biased single-ended and differential high-gain amplifiers based on p-channel organic thin-film transistors and thin-film carbon resistors. The effect of mobility degradation due to aging is reduced from 43% to 2.7% during two months. The bias-point instability due to bias-stress-induced threshold voltage shifts, is limited to 9.6%. The circuits become nearly insensitive to light. Single-ended and differential self-biased amplifiers with resistive load and bias circuitry are implemented having a gain of 29.4 dB and 23.1 dB and a gain-bandwidths of 6.9 kHz and 2.4 kHz, respectively. An input-referred offset of 2mV is achieved.

Keywords: Organic Electronics, Flexible Electronics, Aging, Bias-Stress, Parameter Variation, Organic Thin-Film-Transistor, Organic Amplifier, Self-Biased

11-5

12:10 PM - 12:35 PM

An Encryption-Authentication Unified a/D Conversion Scheme for IoT Sensor Nodes

Vinod Gadde, Hiromitsu Awano, Makoto Ikeda

The University of Tokyo, Japan

Abstract:

Widely distributed sensors, in the IoT era, are vulnerable to attacks, including data sniffing and spoofing. Tamper resistance, data encryption and authentication, which are essential aspects of security of all IoT devices, are becoming ever more critical. We have proposed an Analog-to-Digital Conversion scheme, based on slope A/D conversion, involving two randomized slopes, to realize resistance to side channel

attacks and perform data encryption-authentication during the A/D conversion process. We have designed and fabricated the proposed encryption-authentication unified ADC in 0.18 μ m CMOS process and demonstrated an ENOB of 7.64 bits, DNL = \pm 0.6 LSBs and INL = \pm 0.5/-0.4 LSBs at 24KS/s.

Keywords: An Encryption-Authentication Unified a/D Conversion Scheme for IoT Sensor Nodes

Session	MEM 12: Intelligent Memory System
Date / Time	November 7, 2018 (Wednesday) / 10:30 AM - 12:35 PM
Room	West Gate, B1F
Chair	Tony T. Kim, Nanyang Technological University
Co-Chair	Shyh-Shyuan Sheu, Yuan Ze University

12-1

10:30 AM - 10:55 AM

A 28nm 320Kb TCAM Macro with Sub-0.8ns Search Time and 3.5+x Improvement in Delay-Area-Energy Product Using Split-Controlled Single-Load 14T Cell

Cheng-Xin Xue², Wei-Cheng Zhao², Tzu-Hsien Yang², Yi-Ju Chen², Hiroyuki Yamauchi¹, Meng-Fan Chang²
¹Fukuoka Institute of Technology, Japan; ²National Tsing Hua University, Taiwan

Abstract:

This work proposes a Split-Controlled Single-Load (SCSL) 14T TCAM cell to achieve (1) compact cell area, (2) reduced search delays and energy, (3) less leakage current. A 320Kb 14T-TCAM macro was fabricated using a 28nm CMOS process and modified foundry compact-area 6T cell. The resulting macro lowered search delays to just 710ps and gained a 3.5+x improvement in the figure-of-merit (delay-area-energy product), compared to conventional 16T TCAMs.

Keywords: TCAM、SRAM

12-2

10:55 AM - 11:20 AM

8 A 6.8TOPS/W Energy Efficiency, 1.5μW Power Consumption, Pulse Width Modulation Neuromorphic Circuits for Near-Data Computing with SSD

Kota Tsurumi, Kenta Suzuki, Ken Takeuchi
 Chuo University-Takeuchi Laboratory, Japan

Abstract:

This paper proposes Pulse Width Modulation Neuromorphic (PWMNM) circuits for near-data computing with SSD. A mimicked-neuron in PWMNM consists of 10 pairs of oscillators, clock counters, micro controller and charge pump. PWMNM achieves high energy efficiency and low power consumption, thanks to matrix product operations are processed with number of output pulses as a function of the time instead of conventional current or voltage operation. Both PWMNM and peripheral circuits of NAND flash memory are fabricated with a 180nm standard CMOS process within SSD. Character recognition system is demonstrated by using PWMNM, and the recognition accuracy of 93.3% is achieved.

Keywords: Neuromorphic, Pulse width modulation, Oscillator, Charge pump, Low power consumption, Near-data computing

12-3 (Short Paper)**11:20 AM - 11:32 AM****A 28nm FD-SOI 4KB Radiation-hardened 12T SRAM Macro with 0.6 ~ 1V Wide Dynamic Voltage Scaling for Space Applications**

Ik-Joon Chang, Le Dinh Trang Dang, Dongkyu Seo, Jin-Woo Han, Jinsang Kim
Kyunghee University, Korea

Abstract:

We present a soft-error immune 12T SRAM cell for space applications, namely we-Quatro, and design a 4KB radiation-hardened macro of this SRAM in 28nm FD-SOI. Previously, 10T Quatro has been considered promising for this purpose, however suffers from extremely poor writability under parametric variations. Despite of two more transistors, we-Quatro delivers the same cell area as Quatro. Our simulations and measurements show that our 4KB macro provides robust read and write stabilities for wide supply voltage range of 0.6~1V. More critically, the measured soft-error resilience of we-Quatro is comparable to that of Quatro, significantly better than that of 6T SRAM.

Keywords: Wide Dynamic, Voltage Scaling, Space Applications

12-4 (Short Paper)**11:32 AM - 11:45 AM****Nonvolatile Crossbar 2D2R TCAM with Cell Size of 16.3 F2 and K-Means Clustering for Power Reduction**

Keji Zhou¹, Xiaoyong Xue¹, Jianguo Yang¹, Xiaoxin Xu², Hangbing Lv², Mingyu Wang¹, Ming?췔 Jing¹, Xiaoyang Zeng¹, Steve S. Chung³, Jing Li⁴, Ming Liu²

¹*Fudan University, China*; ²*Institute of Microelectronics of the Chinese Academy of Sciences, China*;

³*National Chiao Tung University, Taiwan*; ⁴*University of Wisconsin-Madison, United States*

Abstract:

A 28nm 16Kb nonvolatile ternary content addressable memory (nvTCAM) test chip based on logic-compatible resistive memory (ReRAM) is demonstrated with high density and low power for packet routing in network applications. The crossbar array exhibits a smallest cell size of 16.3F2 by using 2-diode-2-ReRAM (2D2R) nvTCAM cell, useful for further 3-dimension (3D) stacking. K-means clustering is employed to allocate the storage of routing table entry for given bank count. Then the search of destination IP address can be classified and confined to a specific bank, reducing active banks for power saving. Evaluations show >3X improvement in cell density and >70% reduction in search energy with limited overhead in silicon area for bank count of four. The measured search delay achieves 2ns at nominal supply voltages.

Keywords: TCAM, 2D2R, Crossbar, Machine Learning, K-means Clustering

12-5**11:45 AM - 12:10 PM****An Enhanced Built-Off Test Transceiver with Wide-Range, Self-Calibration Engine for 3.2 Gb/S/Pin DDR4 SDRAM**

Joung-Wook Moon
Samsung Electronics, Korea

Abstract:

This paper presents a wide-frequency-range, self-calibrating, built-off-test (BOT) transceiver for a DDR4 SDRAM interface. The proposed BOT transceiver consists of a data transceiver, a phase-locked loop, a

delay-locked loop, a self-timing calibration (STC) circuit with a 90-degree phase shifter, and a self-voltage calibration (SVC) circuit. In particular, with both the STC and SVC circuits, data channel skew is effectively compensated, and the voltage margin can be maximized while the DDR4 SDRAM is communicating with the test equipment. The BOT transceiver is realized in 20-nm DRAM CMOS technology. Using the fabricated BOT transceiver, we have successfully demonstrated 3.2-Gb/s/pin testing for DDR4 SDRAM with a 1.0-V supply voltage.

Keywords: DDR4 SDRAM, Built-off Test

12-6

12:10 PM - 12:35 PM

An Ultra-Low Power 8T SRAM with Vertical Read Word Line and Data Aware Write Assist

Lu Lu, Taegeun Yoo, Van Loi Le, Tony Tae-Hyoung Kim

NTU, Singapore

Abstract:

This paper presents an 8T SRAM macro with vertical read word line (RWL) and selective dual split power line techniques. The proposed vertical RWL reduces dynamic power consumption during read operation by charging and discharging only selected read bitlines (RBLs). The data-aware dual split power line enhances the write margin (WM) and the static noise margin (SNM) after combined with vertical write bitlines. The 16kb SRAM test chip in 65nm CMOS technology demonstrates the minimum energy consumption of 0.506 pJ at 0.4 V, and the minimum operating voltage of 0.26 V.

Keywords: vertical read word line, data-aware, SRAM, low leakage, low power

Session	DCS 13: Circuit Technologies for Security Enhancement
Date / Time	November 7, 2018 (Wednesday) / 10:30 AM - 12:35 PM
Room	East Gate, B1F
Chair	Koyo Nitta, NTT
Co-Chair	Tsung-Te Liu, National Taiwan University

13-1

10:30 AM - 10:55 AM

A 0.46V-1.1V Transition-Detector with in-Situ Timing-Error Detection and Correction Based on Pulsed-Latch Design in AES Accelerator

Xinchao Shang¹, Weiwei Shan¹, Jiaming Xu¹, Minyi Lu¹, Yiming Xiang², Longxing Shi¹, Jun Yang¹

¹Southeast University, China; ²Spreadtrum Communications, China

Abstract:

To overcome the minimum-delay constraint of latch based error detection and correction (EDAC) techniques, we propose a technique of using pulse latch and transition detector (TD). This method is also advantageous in no need of error recovery by time-borrowing characteristics of the latch. To detect timing violations and minimize the area overhead, we design a quick-response 15-transistor transition detector cover a wide-voltage range from near-threshold voltage (NTV) to Super-V_{th}. Test chips are fabricated in 28nm CMOS process. Silicon measurements demonstrate that the whole design has achieved up to 64.3% energy saving with 180mV additional voltage scaling, compared to the conventional worst-case design at the expense of 4.3% area overhead.

Keywords: Error detection and correction (EDAC) pulse latch transition detector time-borrowing

13-2

10:55 AM - 11:20 AM

Ultra-Lightweight 548 – 1080 Gate 166Gbps/W – 12.6Tbps/W SIMON 32/64 Cipher Accelerators for IoT in 14nm Tri-Gate CMOS

Himanshu Kaul, Mark Anders, Sanu Mathew, Vikram Suresh, Sudhir Satpathy, Amit Agarwal, Steven Hsu, Ram Krishnamurthy

Intel Corporation, United States

Abstract:

A family of 32b data/64b key SIMON cipher accelerators, each reconfigurable for encrypt/decrypt modes and fabricated in 14nm tri-gate CMOS, is optimized for a range of area and performance targets: (i) a 1080-gate one round/cycle design occupying 136 μ m² die area uses reconfigurable circuits for forward/reverse key generation, (ii) a 752-gate 16 cycles/round bit-serial design with a single round/key logic bit-slice lowers layout area by 38% to 85 μ m², and (iii) latch-based key/text storage for the bit-serial circuit reduces area further by 22% to 66 μ m² at 272 cycles/round for a 548-gate design with measured 11.4Mbps, 209 μ W, 750mV operation. Ultra-low voltage circuit optimizations enable peak energy efficiency from 166Gbps/W at 380mV for the bit-serial latch-based design to 12.6Tbps/W at 260mV for the parallel, one round/cycle design.

Keywords: SIMON cipher, ultra-lightweight, encryption, IoT

13-3

11:20 AM - 11:45 AM

31.3 Us/Signature-Generation 256-Bit Fp ECDSA Crypto Processor

Hiromitsu Awano², Makoto Ikeda¹

¹The University of Tokyo, Japan; ²VLSI Design and Education Center, Japan

Abstract:

A 256-bit Fp ECDSA crypto processor featuring low latency, low energy consumption and capability of changing the Elliptic curve parameters is designed and fabricated in SOTB 65nm CMOS process. We have demonstrated the lowest ever reported signature generation time of 31.3 us. Energy consumption is 3.28 uJ/signature-generation, which is same as the lowest reported till date.

Keywords: ASIC, SOTB, ECDSA, V2V communications, IoT

13-4

11:45 AM - 12:10 PM

A Physically Unclonable Function with 0% BER Using Soft Oxide Breakdown in 40nm CMOS

Kai-Hsin Chuang², Erik Bury¹, Robin Degraeve¹, Ben Kaczer¹, Dimitri Linten¹, Ingrid Verbauwhede²

¹imec, Belgium; ²KU Leuven, Belgium

Abstract:

A physically unclonable function (PUF) utilizing the randomness of soft oxide breakdown (BD) locations in MOSFETs is presented. The so-called soft-BD PUF features a self-limiting mechanism to generate one single soft-BD spot in a pair of MOSFETs; the subsequent BD location is used as the source of entropy to generate a highly stable "0" or "1" bit with an equal probability of 0.5. The soft-BD PUF comprising all the essential periphery circuits are fabricated in a 40nm CMOS process. Experiments on the test chips show that the PUF has no instability in most operating conditions using the proposed readout scheme. The native bit error rate remains zero from VDD=0.8V to 1.5V at room temperature and from -20°C to 120°C at nominal VDD=0.9V. The throughput is shown to be at least 40 Mb/s and the PUF readout consumes only 51.8 fJ/bit. The randomness and uniqueness of the PUF are close to an ideal case, and no spatial correlation was observed.

Keywords: physically unclonabl function, key generation, soft breakdown, stability

13-5

12:10 PM - 12:35 PM

A 373F^2 2D-Power-Gated EE SRAM Physically Unclonable Function with Dark-Bit Detection Technique

Kunyang Liu, Yue Min, Xuan Yang, Hanfeng Sun, Hirofumi Shinohara

Waseda University, Japan

Abstract:

This paper presents an Enhancement-Enhancement (EE) SRAM physically unclonable function (PUF) with a dark-bit masking technique based on an integrated VSS-bias generator. The EE SRAM cell improves native stability to 0.21% bit-error-rate (BER). For stability ensuring, bit-cells that are potentially unstable due to environmental variations or aging are detected with a lightweight bias generator. Measurement results of ten prototype chips fabricated in 130nm CMOS show that after masking the detected dark bits, 1.3E-6 BER is achieved across -40-120°C/0.8-1.4V VT-corners. The NMOS-only bit-cell is highly compact (373F^2). A 2D-power-gating technique is applied for low-power and high attack-tolerance.

Keywords: physically unclonable function (PUF), dark-bit masking, EE SRAM, IoT, hardware security

Session	ACS 14: Inductive DC-DC Converters
Date / Time	November 7, 2018 (Wednesday) / 1:40 PM - 3:20 PM
Room	North Gate, B1F
Chair	Hyun-Sik Kim, Dankook University
Co-Chair	Takeshi Ueno, Toshiba Corporation

14-1

1:40 PM - 2:05 PM

An 82.1%-Power-Efficiency Single-Inductor Triple-Source Quad-Mode Energy Harvesting Interface with Automatic Source Selection and Reversely Polarized Energy Recycling

Chih-Lun Lo, Hao-Chung Cheng, Pei-Chun Liao, Yi-Lun Chen, Po-Hung Chen
National Chiao Tung University, Taiwan

Abstract:

A single-inductor triple-source quad-mode energy harvesting interface with automatic source selection is designed for multi-source energy harvesting. It operates at harvesting mode (HM), recycling mode (RM), storage mode (SM), and backup mode (BM) automatically according to input and load conditions. The proposed reversely polarized energy recycling (RPER) technique extends the available output power range by 10x with 25.3% efficiency improvement. The proposed interface achieves the peak efficiency of 82.1%.

Keywords: energy harvesting, automatic source selection, reversely polarized energy harvesting

14-2

2:05 PM - 2:30 PM

A Transient-Enhanced Constant on-Time Buck Converter with Light-Load Efficiency Optimization

Mao-Ling Chiu, Tzu-Hsuan Yang, Tsung-Hsien Lin
National Taiwan University, Taiwan

Abstract:

Two key challenges in designing regulators of handheld devices are load transient time and light-load efficiency. A conventional constant on-time (COT) buck converter is often adopted for its simple architecture facilitates a fast response with good light-load efficiency. To further enhance these design issues, two techniques are proposed in this work. One is the transient-enhanced (TE) technique which can reduce the settling time and minimize the voltage dips. The other one is the self-tuning technique to implement light-load efficiency optimization, termed as the near-optimal reverse current calibration (NORCC). Measurement results demonstrate settling time and undershoot voltage of 960 ns and 50 mV, respectively, during the load changes from 100 mA to 1.5 A. The efficiency is better than 79% from 10 mA to 1.7 A; the peak value is 93.6% at 300 mA load current.

Keywords: DC-DC converter, Constant on-time control

14-3 (Short Paper)**2:30 PM - 2:42 PM****A 99.2% Tracking Accuracy Single-Inductor Quadruple-Input-Quadruple-Output Buck-Boost Converter Topology with Periodical Interval Perturbation and Observation MPPT**

Ke-Horng Chen

*EE, National Chiao Tung University, Taiwan***Abstract:**

this paper provides a Single-Inductor Quadruple-Input-Quadruple-Output buck-boost converter to achieve maximum tracking efficiency of 99.2% due to continuous supply in one cycle. The Maximum Power Point (MPP) tracking mode and the Harvest Energy Delivering (HED) mode harvest each energy harvesting source, deliver energy to the battery and supply it to the loading system in one cycle. Each output voltage ranges from 600mV to 2.5V and the maximum output power is up to 60mW. The peak efficiency is 91.2%.

Keywords: Single-Inductor Quadruple-Input-Quadruple-Output (SI-QIQO), Maximum Power Point Tracking (MPPT), Harvest Energy Delivering (HED)

14-4 (Short Paper)**2:42 PM - 2:55 PM****A Digital Multiphase Converter with Sensor-Less Current and Thermal Balance Mechanism**

Yu-Sin Chen, Kai-Yu Hu, Chien-Hung Tsai

*National Cheng-Kung University, Taiwan***Abstract:**

This paper presents a sensor-less approach to achieve current balance and thermal balance in a digital voltage mode controlled four-phase buck converter. Instead of using current sensors and temperatures sensor to obtain the current and thermal information as most of previous researches, the sensor-less equivalent resistance ratio estimation is used in this work. The digital controller was manufactured by TSMC 0.18- μ m 1P6M standard CMOS process. The experimental results are attached. The current balance scheme improves the current sharing error from 35% to 6.3%, while the thermal balance technique narrows down the peak temperature difference from 6.6 to 1.8 degrees Celsius.

Keywords: Multiphase buck converter, Digitally-controlled, Current balance, Thermal balance, Duty disturbance

14-5**2:55 PM - 3:20 PM****A Fully-Integrated LC-Oscillator Based Buck Regulator with Autonomous Resonant Switching for Low-Power Applications**

Tianyu Jia, Jie Gu

*Northwestern University, United States***Abstract:**

In this paper, a fully integrated, LC-oscillator based buck regulator is presented for low power applications. The proposed design uses a self-resonator as both high-speed clock source and a resonant switch driver for the regulator, which not only achieves significantly improved energy efficiency at 2GHz switching frequency but also delivered a high-quality clock source eliminating requirement of the external high-speed clocks. Measurement on a 65nm testchip shows a wide tuning range from 0.35V to 0.82V with an

input voltage 1.1V. The proposed design achieves a peak efficiency of 70.3% and an autonomous clock-less operation. The regulator core area is only 0.079mm².

Keywords: Buck regulator, fully integrated, input-clock free, resonant switching, low power applications

Session	DCS 15: Energy-Efficient Circuits and Architectures
Date / Time	November 7, 2018 (Wednesday) / 1:40 PM - 3:20 PM
Room	South Gate, B1F
Chair	Massimo Alioto, National University of Singapore
Co-Chair	Tay-Jyi Lin, National Chung Cheng University Yoonmyung Lee, Sungkyunkwan University

15-1

1:40 PM - 2:05 PM

A Bulk 65nm Cortex-M0+ SoC with All-Digital Forward Body Bias for 4.3X Subthreshold Speedup

Pranay Prabhat², Graham Knight², Supreet Jeloka¹, Sheng Yang², James Myers²

¹Arm Inc., Austin, US., United Kingdom; ²Arm Ltd, Cambridge, UK., United Kingdom

Abstract:

IoT devices demand ultra-low power operation while still achieving the performance demanded by application constraints. Dynamic forward body biasing can help to achieve this by providing a speed-up during active operation without incurring a leakage penalty during standby periods. At subthreshold voltage levels, the Low Voltage Swapped Body (LVSB) technique, in which n-well and p-well are driven to VSS and VDD respectively, gives a significant speedup. This work presents key advances to leverage LVSB, proven on a bulk 65nm subthreshold Arm Cortex-M0+ system. The system achieves a 4.3X speedup at a cost of only 11% average power and 10.4% area.

Keywords: Arm, Cortex-M0+, LVSB, subthreshold, IoT, FBB

15-2

2:05 PM - 2:30 PM

A 2.1 pJ/Bit, 8 Gb/S Ultra-Low Power in-Package Serial Link Featuring a Time-Based Front-End and a Digital Equalizer

Po-Wei Chiu, Muqing Liu, Qianying Tang, Chris H. Kim

University of Minnesota, United States

Abstract:

A TDC based receiver with TBFE is demonstrated on in-package serial link in 65nm GP process. A highly linear TA is proposed to amplify the small time difference generated from VTC. A BER less than 10E-12 is verified using the in-situ measurement circuits. Our proposed TBFE is highly digitalized, low voltage operation and has good compatibility with post digital circuit. The compact size and high energy efficiency show that the proposed time-based receiver is promising for SiP applications.

Keywords: Time-based, digital equalization, time-to-digital converter (TDC), system-in-package (SiP), digital intensive, inverter-based

15-3 (Short Paper)**2:30 PM - 2:42 PM****A 2.69 Mbps/mW 1.09 Mbps/kGE Conjugate Gradient-Based MMSE Detector for 64-QAM 128*8 Massive MIMO Systems**

Guiqiang Peng, Leibo Liu, Qiushi Wei, Yao Wang, Shouyi Yin, Shaojun Wei
Tsinghua University, China

Abstract:

This paper proposes a VLSI architecture for an MMSE detector in an uplink 128*8 64-QAM massive MIMO system to achieve high energy and area efficiencies. A soft-output recursion conjugate gradient (RCG)-based minimum mean square error (MMSE) detector is fabricated onto a 3.5mm² silicon with TSMC 65nm CMOS technology for a 64-QAM 128*8 massive MIMO system. The chip achieves a 1.5Gbps throughput under a 500MHz working frequency while dissipating 557mW at 1.2V. The energy efficiency (throughput/power) and area efficiency (throughput/area) are 2.69Mbps/mW and 1.09Mbps/kGE, which are 2.39-to-2.47* and 1.15-to-8.81* those of the normalized state-of-the-art designs, respectively.

Keywords: Massive MIMO detection, minimum-mean-square-error (MMSE), recursion conjugate gradient, VLSI, wireless communication

15-4 (Short Paper)**2:42 PM - 2:55 PM****A Fully Standard-Cell Based on-Chip BTI and HCI Monitor with 6.2x BTI Sensitivity and 3.6x HCI Sensitivity at 7 nm Fin-FET Process**

Mitsuhiko Igarashi, Yuuki Uchida, Yoshio Takazawa, Yasumasa Tsukamoto, Koji Shibutani, Koji Nii
Renesas Electronics Corporation, Japan

Abstract:

We propose an on-chip NBTI, PBTI and HCI monitor by using standard cell based unbalanced RO at 7 nm Fin-FET process. The NBTI monitor consists of two ROs; one is NBTI sensitive RO (NBTI-RO) and the other is R-NBTI-RO with reversed cell order of NBTI-RO. R-NBTI-RO gets fast after NBTI stress where as other ROs is degraded. As a result, 6.2x NBTI sensitivity compared with normal inverter based RO (INV-RO) and negligibly small PBTI sensitivity are achieved. PBTI monitor is achieved in a similar manner. In HCI monitor, HCI degradation is 3.6x emphasized by simulating worst-case waveform of logic circuit by using unbalanced drive strength configuration of INV cell. The measurement result of our test chip fabricated in 7 nm Fin-FET process shows that measured result of each RO is well matched to the simulation one. These high sensitive NBTI/PBTI/HCI monitor can be a solution to optimize required GB in a field, detect variations and outliers of aging at time of testing to achieve both high performance and high reliability of autonomous driving LSI.

Keywords: NBTI, PBTI, HCI, Standard Cell based, Ring Oscillator, Unbalanced, 7 nm FinFET technology, Guardband

A 140 nW, 32.768 KHz, 1.9 ppm/°C Leakage-Based Digitally Relocked Clock Reference with 0.1 ppm Long-Term Stability in 28nm FD-SOI

Guénolé Lallement³, Fady Abouzeid², Thierry Di Gilio², Philippe Roche², Jean-Luc Autran¹

¹Aix-Marseille University, France; ²ST Microelectronics, France; ³ST Microelectronics / Aix-Marseille University, France

Abstract:

The design of Ultra-Low Power clock reference systems with highly energy-efficient operations is a key concept to achieve autonomous Internet-of-Things applications. In this work, a System-on-Chip is presented, embedding an area-efficient ultra-low voltage clock reference generator built on a digitally controlled leakage-based Ring Oscillator. Through a relocking scheme using a 2²² Hz external quartz reference, an associated digital compensation circuit ensures a stable output frequency of 32.768 kHz over inherent Process, Voltage and Temperature variations. The whole design has been fabricated in 28 nm FD-SOI technology and operates at a fixed supply voltage V_{dd} of 0.5V. By combining Ultra-Low Power techniques, a 15 nW power consumption is achieved for the Oscillator and 125 nW for the digital compensation. The circuit area of the proposed clock source is 56.2 μm x 29.1 μm. A 90 ppm/V voltage accuracy has been measured over 10 packaged dies for V_{dd} ± 8%. A temperature accuracy of 1.9 ppm/°C is also reported from 0°C to 50°C. Lastly, the long-term frequency stability is characterized by an Allan deviation floor of 0.1 ppm.

Keywords: Ultra-Low Power, Timer, Oscillator, Digital Compensation, 28nm FD-SOI

Session	WLN 16: Advanced Wireline Equalization
Date / Time	November 7, 2018 (Wednesday) / 1:40 PM - 3:20 PM
Room	West Gate, B1F
Chair	Wei-Zen Chen, National Chiao-Tung University
Co-Chair	Young-Chan Jang, Kumoh National Institute of Technology

16-1

1:40 PM - 2:05 PM

A 2× Blind Oversampling FSE Receiver with Combined Adaptive Equalization and Infinite-Range Timing Recovery

Seuk Son², Hwanseok Yeo¹, Sigang Ryu², Jaeha Kim²

¹Samsung electronics, Korea; ²Seoul national university, Korea

Abstract:

A 2× blind-oversampling, fractionally-spaced equalizer (FSE) receiver is presented as an effective way to combine adaptive equalization and infinite-range timing recovery. A FSE can perform equalization as well as timing adjustment via data-interpolation and the presented work demonstrates an infinite-range timing recovery using a set of two half-UI-spaced, 4-tap FSEs that seamlessly switch across the UI boundaries. A current-integrating summer and multi-input regenerative latch help the 4-tap FSEs and 4-tap DFEs achieve low power dissipation, respectively. A prototype receiver fabricated in a 28nm CMOS consumes 3.5pJ/bit and 0.10mm² at 9Gb/s while compensating a 22-dB channel loss and a 100ppm frequency offset between the transmitted data and blind sampling clocks.

Keywords: wireline, receiver, CDR, adaptive equalizer, fractionally-spaced-equalizer, decision-feedback-equalizer

16-2

2:05 PM - 2:30 PM

A Bimodal (NRZ/PAM-4) ISI Tolerant Timing Recovery with Adaptive DDJ Equalization

Masum Hossain², . Aurangozeb², Nhat Nguyen¹

¹Rambus Inc, Sunnyvale, United States; ²University of Alberta, Canada

Abstract:

This paper describes low latency bimodal NRZ/PAM-4 timing recovery. This scheme reduces latency and power consumption by eliminating the need for data equalization in the timing recovery path. Rather it directly equalizes the data dependent jitter by adaptively shifting the ISI effected zero crossings. The implemented prototype in 65nm CMOS supports both 10 Gb/s NRZ and 20 Gb/s PAM-4 consuming only 23 mW. The CDR achieves fbaud/500 peaking free tracking bandwidth and achieves superior jitter tolerance for both PAM-4 and NRZ.

Keywords: Clock and Data Recovery, DDJ Equalization, Timing adaptation, Digital receiver timing recovery

16-3

2:30 PM - 2:55 PM

A 12-Gb/s AC-Coupled FFE TX with Adaptive Relaxed Impedance Matching Achieving Adaptation Range of 35-75 Ω Z0 and 30-550 Ω RRX

Minsoo Choi, Myungguk Lee, Byungsub Kim

Pohang University of Science and Technology (POSTECH), Korea

Abstract:

A 12-Gb/s FFE TX which automatically adapts to arbitrary impedances of AC-coupled channels and RXs is proposed. The TX detects impedances of the channel and the RX within 8% and 5% errors, respectively, and adaptively relaxes its impedance matching to maximize eye size at cost of a negligible penalty in signal integrity. In experiment, the TX adapted to any combination of a channel impedance of 35-75 Ω and an RX impedance of 30-550 Ω while achieving eye size larger than the conventional TX with impedance matching. At most, a completely closed eye was increased to 136mV by the proposed TX.

Keywords: AC-coupled interconnects, feed forward equalization, impedance adaptation, impedance matching, relaxed impedance matching

16-4

2:55 PM - 3:20 PM

A 40 Gb/s PAM-4 Receiver with 2-Tap DFE Based on Automatically Non-Even Level Tracking

Chia-Tse Hung, Yu-Ping Huang, Wei-Zen Chen

National Chiao Tung University, Taiwan

Abstract:

A 40 Gb/s PAM-4 receiver comprised of a continuous-time linear equalizer (CTLE) and 2-tap decision-feedback equalizers (DFE) based on a novel level tracking circuit (ANLT) is proposed. A sign-sign LMS engine is embedded for the DFE and ANLT coefficients adaptation to accommodate different channel loss. The ANLT is capable of automatically tracking a non-evenly spaced PAM-4 signal, allowing the receiver to demodulate a distorted input with 2-bit flash ADCs. Fabricated in a TSMC 40nm CMOS technology, the whole receiver consumes 250.8mW at 40 Gb/s operation. Core area is 0.274 mm².

Keywords: PAM, CTLE, DFE, automatically non-even level tracking (ANLT), sign-sign least mean square (SS-LMS)

Session	RF 17: Oscillators and Synthesizers
Date / Time	November 7, 2018 (Wednesday) / 1:40 PM - 3:20 PM
Room	East Gate, B1F
Chair	Minjae Lee, Gwangju Institute of Science and Technology
Co-Chair	Satoshi Tanaka, Murata

17-1

1:40 PM - 2:05 PM

A 1.6-GHz 3.3-mW 1.5-MHz Wide Bandwidth $\Delta\Sigma$ Fractional-N PLL with a Single Path FIR Phase Noise Filtering

Jingcheng Tao, Chunhuat Heng

National University of Singapore, Singapore

Abstract:

This paper describes a novel $\Delta\Sigma$ quantization noise filtering method for wideband $\Delta\Sigma$ fractional-N PLL. A single path finite impulse response (FIR) filtering technique is realized through two-step phase interpolation. A prototype 1.6 GHz $\Delta\Sigma$ fractional-N PLL with 1.5 MHz wide loop bandwidth is implemented in 130-nm CMOS process. Measurement results show that the proposed technique effectively reduces the high frequency quantization noise by 12 dB and achieves an in-band phase noise of -101 dBc at 400 kHz and 2.14ps integrated jitter, while consuming only 3.3 mW power and an area of 0.24mm².

Keywords: wideband, fractional-N PLL, FIR, single path, phase noise filtering

17-2

2:05 PM - 2:30 PM

A 37-GHz-Input Divide-by-36 Injection-Locked Frequency Divider with 1.6-GHz Lock Range

Sangyeop Lee, Kyoya Takano, Ruibing Dong, Shuhei Amakawa, Takashi Yoshida, Minoru Fujishima

Hiroshima University, Japan

Abstract:

This paper presents a divide-by-36 injection-locked frequency divider (ILFD). It locks on to a 37-GHz input over a locking range of about 1.6GHz (4.3%) and outputs approximately 1 GHz, which is low enough for further division by a programmable divider. The high division ratio is realized by time-gating the superharmonic input signal and injecting it into a 9-stage ring VCO at 9 feeding points. Nine gating signals are generated by the ring VCO itself by logic operation such that the input signal is injected only during the right time slice for each of the feeding points.

Keywords: Injection-locked frequency divider (ILFD), lock range, ring VCO, CMOS

17-3 (Short Paper)

2:30 PM - 2:42 PM

A 37.5-45.1GHz Superharmonic-Coupled QVCO with Tunable Phase Accuracy in 28nm Bulk CMOS

Luya Zhang¹, Ali Ameri¹, Yi-An Li¹, Nai-Chung Kuo¹, Mekhail Anwar², Ali Niknejad¹

¹University of California, Berkeley, United States; ²University of California, San Francisco, United States

Abstract:

This paper presents the design and measurements of a new super-harmonic coupled millimeter-wave (mmW) quadrature VCO. The mechanism of using super-harmonic coupling to ensure quadrature locking and its capability of rejecting phase error is analyzed. Based on the analysis, a new super-harmonic coupling structure is proposed, which can adjust quadrature error against mismatch to satisfy practical system requirements. For verification, a 40GHz QVCO is implemented in 28nm bulk CMOS. The measurement shows a frequency coverage from 37.5GHz to 45.1GHz with 8.4mW power consumption and 0.18 degree quadrature error.

Keywords: CMOS, millimeter-wave, quadrature VCO, superharmonic coupling, phase accuracy

17-4 (Short Paper)

2:42 PM - 2:55 PM

A Fast Auto-Frequency Calibration Technique for Wideband PLL with Wide Reference Frequency Range

Zhao Zhang, Jincheng Yang, Liyuan Liu, Nan Qi, Peng Feng, Jian Liu, Nanjian Wu

Institute of Semiconductors, Chinese Academy of Sciences, China

Abstract:

This paper proposes a fast auto frequency calibration (AFC) technique for wideband PLL with wide reference frequency range. The AFC circuit block adopts a proposed clock controller and a current-mode logic (CML) divider-by-2 divider to accelerate the AFC process without the penalty of AFC resolution. It also adopts the adjustable AFC counting period technique to speed up the AFC process at low reference frequency and to reduce AFC time variation within wide frequency range of reference clock. A 0.1~5 GHz $\Delta\Sigma$ fractional-N PLL with this AFC technique is designed and implemented in 65-nm CMOS process. The measurement results show that in the reference frequency range from 15 to 50 MHz, the AFC time varies only from 1.25 to 1.86 μ s with AFC resolution range from 3 to 5 MHz.

Keywords: Fast AFC, AFC resolution, PLL, wide reference frequency range

17-5

2:55 PM - 3:20 PM

A Sub-Picosecond Hybrid DLL for Large-Scale Phased Array Synchronization

Matan Gal-Katziri, Ali Hajimiri

California Institute of Technology, United States

Abstract:

A large-scale timing synchronization scheme for scalable phased arrays is presented. This approach utilizes a DLL co-designed with a subsequent 2.5GHz PLL. The DLL employs a low noise, fine/coarse delay tuning to reduce the in-band rms jitter to 323fs, an order of magnitude improvement over previous works at similar frequencies. The DLL was fabricated in a 65nm bulk CMOS process and was characterized from 27MHz to 270MHz. It consumes up to 3.3mW from a 1V power supply and has a small footprint of 0.036mm².

Keywords: CMOS integrated circuits, phased-arrays, radio frequency, tracking loops, delay-lines, phase locked loops, phase noise

Session	DC 18: ADCs and Calibration Techniques
Date / Time	November 7, 2018 (Wednesday) / 3:50 PM - 5:55 PM
Room	North Gate, B1F
Chair	Chih-Cheng Hsieh, National Tsing Hua University
Co-Chair	Zule Xu, University of Tokyo

18-1

3:50 PM - 4:15 PM

A 7b 2 Gs/S Time-Interleaved SAR ADC with Time Skew Calibration Based on Current Integrating Sampler

Wenning Jiang², Yan Zhu², Chi-Hang Chan², Boris Murmann¹, Seng-Pan U², Rui Paulo Martins²

¹stanford university, United States; ²university of macau, Macau

Abstract:

This paper presents a time-interleaved (TI) SAR ADC that utilizes the characteristic of the current integrating (CI) sampler for sampling time skew background calibration, while it also provides buffering and anti-aliasing filtering functions, simultaneously. The inter-sample interaction in the CI sampler enables the mapping of the time domain information to the amplitude domain. Time skew errors can therefore be extracted by comparing the output-code variance among channels without requiring a reference path. A 2-channel 2 GS/s 7b TI-SAR prototype realized in 28-nm CMOS achieves a 36.4 dB SNDR at Nyquist with >2.6 GHz ERBW after calibration. The ADC with CI sampler consumes 7.62 mW, leading to a Walden FoM of 70.8 fJ/conversion-step.

Keywords: Time-interleaved ADC, current integrating sampler, background calibration, timing skew.

18-2

4:15 PM - 4:40 PM

A 15.1-mW 6-Gs/S 6-Bit Flash ADC with Selectively Activated 8x Time-Domain Interpolation

Il-Min Yi, Naoki Miura, Hiroyuki Fukuyama, Hideyuki Nosaka

NTT Coporation, Japan

Abstract:

A selectively activated 8x time-domain interpolation is proposed for a low-power high-speed 6-bit flash ADC. By improving the linearity of the voltage-to-time conversion gain, a 3-bit resolution is achieved in time-to-digital conversion. Hence, the number of the dynamic comparators is reduced from conventional 63 to 10. Also, unlike other time-domain interpolation schemes, time-to-digital converters are selectively activated to reduce the power consumption of the time-to-digital conversion. The flash ADC fabricated in a 1-V 65-nm CMOS process achieves 6 GS/s with 15.1-mW power consumption. It shows a 31.18-dB SNDR and an 85 fJ/conv.-step FoM with a Nyquist frequency input.

Keywords: ADC, flash ADC, time-domain interpolation, TDC, linearity

18-3 (Short Paper)**4:40 PM - 4:52 PM****A 38-mW 7-Bit 5-Gs/S Time-Interleaved SAR ADC with Background Skew Calibration**

Yung-Hui Chung, Chia-Yi Hu, Che-We Chang

*National Taiwan University of Science and Technology, Taiwan***Abstract:**

This paper presents a 7-bit 5-GS/s time-interleaved SAR ADC with background timing skew calibration. The two-step approaching skew calibration was proposed to reduce the tuning range of the digital control delay circuit, thus suppress the additional clock jitter. The ping-pong domino-SAR ADC architecture was proposed to speed up channel-ADCs. The prototype ADC consumes a total power of 38 mW from a 1.2V supply and occupies an active area of 0.69 mm² in a 55nm low-power CMOS technology. For 10 MHz input, the measured SNDR and SFDR are 42.7 and 65 dB, respectively. The ENOB is 6.8 bits, equivalent to the peak FOM of 69 fJ/conversion-step. At the Nyquist rate, this ADC achieves 35.9 dB SNDR and 45 dB SFDR. The ENOB is 5.7 bits, equivalent to the Nyquist FOM of 150 fJ/conversion-step.

Keywords: ADC, DAC, SAR ADC, skew calibration, time-interleaved ADC

18-4 (Short Paper)**4:52 PM - 5:05 PM****A 0.6-to-1V 10k-to-100kHz BW 11.7b-ENOB Noise-Shaping SAR ADC for IoT Sensor Applications in 28-nm CMOS**

Young-Ha Hwang, Yoonho Song, Jun-Eun Park, Deog-Kyoon Jeong

*Seoul National University, Korea***Abstract:**

This paper presents a noise-shaping SAR ADC for IoT sensor applications. The ADC exploits 2nd-order passive noise-shaping loop without a quiescent current. To reduce harmonic distortion induced by a mismatch between MSBs, thermometer-coded 3-bit MSBs are implemented with a dynamic element matching (DEM) technique. Furthermore, a programmable majority-voting (PMV) technique for LSB decision is applied in order to relax noise requirement of a comparator. With the DEM and PMV, SFDR and SNDR are enhanced by 11.7 dB and 7.4 dB at a 1.0 V supply, respectively. For 50 kHz BW, the modulator dissipates 74.5 μ W from a 1.0 V supply and achieves a peak SNDR of 72.3 dB, a peak SNR of 73.7 dB and a DR of 73.8 dB. The prototype modulator is fabricated in 28 nm CMOS technology, occupying an area of 0.0575 mm².

Keywords: SAR ADC, noise shaping, dynamic element matching, majority voting, scalable bandwidth, IoT sensor.

18-5**5:05 PM - 5:30 PM****A Calibration-Free 0.7-V 13-Bit 10-Ms/S Full-Analog SAR ADC with Continuous-Time Feedforward Cascaded (CTFC) Op-Amps**

Kwuang-Han Chang, Chih-Cheng Hsieh

*National Tsing Hua University, Taiwan***Abstract:**

A calibration-free 13-bit 10-MS/s full-analog SAR ADC integrates the functions of comparator, SAR logic, and DAC switches into multiple inverter-based regenerative amplifiers (IRAs) to have a double timing

budget for settling and relax the bandwidth requirement of analog circuits compared to the conventional SAR ADC. The continuous-time feedforward cascaded (CTFC) Op-amps are proposed to enhance the residue SNR using open-loop low gain-bandwidth amplifiers instead of closed-loop high-precision amplifiers. The prototype in 40nm CMOS occupies 0.013mm² and achieves 67.6dB SNDR, 77.2dB SFDR, 3.2fJ/conv.-step FoMW, and 176.6dB FoMS without any calibration.

Keywords: SAR ADC, high-resolution, calibration-free, full-analog, continuous-time, feedforward cascaded, stability

18-6

5:30 PM - 5:55 PM

An 89.55dB-SFDR 179.6dB-FoMS 12-Bit 1MS/S SAR-Assisted SAR ADC with Weight-Split Compensation Calibration

o-Sheng Hu, Jhao-Huei Lin, Ding-Guo Lin, Kai-Yue Lin, Hsin-Shu Chen

National Taiwan University, Taiwan

Abstract:

This paper presents an 89.55dB-SFDR 2.55μW 12-bit 1MS/s SAR-assisted SAR ADC in 40nm CMOS at 0.7V supply. The proposed weight-split compensation provides an accurate mapping between capacitor mismatch and digital weight to take advantages of both low-power skipping switching method and robust digital calibration. The reconfigurable redundancy region with tracking bits is used to speed up the calibration time to only 112 clock cycles. The SFDR is improved by 19.45dB with unit capacitors of 0.25fF for power-saving. The prototype ADC achieves the SNDR of 69.1dB at Nyquist rate. It results in an FoMS of 179.6dB and an FoMW of 1.43fJ/c.-s.

Keywords: low-power, SAR ADC, SAR-assisted and on-chip capacitor mismatch calibration

Session	DCS+FPGA 19: Multimedia and Signal Processing Hardware
Date / Time	November 7, 2018 (Wednesday) / 3:50 PM - 5:30 PM
Room	South Gate, B1F
Chair	Ji-Hoon Kim, Ewha Womans University
Co-Chair	Byungsub Kim, POSTECH

19-1

3:50 PM - 4:15 PM

An Image Recognition Processor with Time-Domain Accelerators Using Efficient Time Encoding and Non-Linear Logic Operation

Zhengyu Chen, Jie Gu

Northwestern University, United States

Abstract:

This paper presents novel time-domain circuit techniques including double encoding strategy, shared time generator (TG) and bit-scalable design which significantly improve the performance of time-domain signal processing (TDSP) and error tolerance. A feature-extraction and vector-quantization processor accelerated by TDSP has been developed for real-time image recognition. A 55nm prototype chip shows 72 fps/core (@1.33 GHz) operation with significant enhancement from time-domain techniques compared with conventional digital implementation.

Keywords: time-domain signal processing, image recognition, bit-scalable design, double-encoding scheme.

19-2

4:15 PM - 4:40 PM

A 95pJ/Label Wide-Range Depth-Estimation Processor for Full-HD Light-Field Applications on FPGA

Li-De Chen, Yu-Ta Lu, Yu-Ling Hiao, Bo-Hsiang Yang, Wei-Chih Chen, Chao-Tsung Huang

National Tsing Hua University, Taiwan

Abstract:

High-resolution and wide-range depth maps are the key to enable novel light-field applications, such as digital refocusing, view synthesis, and 3D reconstruction. In this paper, we present an energy-efficient depth-estimation processor on FPGA to meet this purpose. There are two major contributions. First, image-guided depth inference and upsampling is adopted and implemented to provide accurate depth maps while lowering the working frequency from 215MHz to 54MHz. Second, octave search range sampling is proposed to efficiently allocate depth labels for wide-depth-range scenes to save computation and maintain accuracy. Finally, the implementation result on Xilinx ZC706 shows ASIC-comparable energy efficiency??5pJ/label??for Full-HD five-view light fields at 30fps.

Keywords: light field, depth estimation, FPGA, Full HD

19-3

4:40 PM - 5:05 PM

A 280mV 3.1pJ/Code Huffman Decoder for Deflate Decompression Featuring Opportunistic Code Skip and 3-Way Symbol Generation in 14nm Tri-Gate CMOS

Sudhir Satpathy, Sanu Mathew, Vikram Suresh, Vinodh Gopal, James Guilford, Mark Anders, Himanshu Kaul, Amit Agarwal, Steven Hsu, Ram Krishnamurthy
Intel Corporation, United States

Abstract:

A 10,790 μ m² dynamic Huffman decoder targeted for DEFLATE header decompression in area and energy constrained IoT platforms is fabricated in 14nm Tri-gate CMOS. Ternary CAM (TCAM) assisted concurrent literal-length and distance tree generation, opportunistic code-skipping with register file tagging to leverage symbol sparsity, and 3-way forward-reverse-parallel Huffman decoding results in 300 cycle header processing latency, 2.4 \times faster than conventional serial decoding approach. Absence of custom circuits enables a fully synthesizable design operating over a wide supply range of 210-900mV with 895M codes/s throughput measured at 750mV, 25°C. Near-threshold voltage operation and clock power reduction with vector latch insertion provides peak energy-efficiency of 3.1pJ/code (5.9 \times higher than nominal) at 280mV, 15MHz operation with 32 μ W and 6 μ W total and leakage power consumption.

Keywords: DEFLATE, Dynamic Huffman Decoder, TCAM

19-4

5:05 PM - 5:30 PM

A Wearable Auto-Patient Adaptive ECG Processor for Shockable Cardiac Arrhythmia

Syed Muhammad Abubakar, Muhammad Rizwan Khan, Wala Saadeh, Muhammad Awais Bin Altaf
Lahore University of Management Sciences (LUMS), Pakistan

Abstract:

A non-machine learning patient-specific shockable cardiac arrhythmia (SCA) classification processor based on single lead electrocardiogram (ECG) is presented. The proposed SCA detection processor integrates a hardware-efficient reduced-set-of-five (RSF5) feature extraction engine to extract SCA and non-SCA, self-adaptive patient-specific threshold engine for the peak and interval detection from the ECG, and simplified decision logic to discriminate the arrhythmia in real-time. The SCAD processor consumes 0.89 μ J/classification while classifying with an average sensitivity, and specificity of 98.7%, and 100%, respectively.

Keywords: cardiac arrhythmia, defibrillator, ecg processor, feature extraction, FPGA, wearable

Session	SOC 20: Intelligent Low-Power SoCs
Date / Time	November 7, 2018 (Wednesday) / 3:50 PM - 5:30 PM
Room	West Gate, B1F
Chair	Pei-Yun Tsai, National Central University
Co-Chair	Daisuke Mizoguchi, Renesas

20-1

3:50 PM - 4:15 PM

A Capacitance-to-Digital Converter Integrated in a 32bit Microcontroller for 3D Gesture Sensing

Mitsuru Hiraki, Sugako Otani, Masao Ito, Takuya Mizokami, Masahiro Araki, Hiroyuki Kondo

Renesas Electronics Corporation, Japan

Abstract:

This paper describes a capacitance-to-digital converter (CDC) integrated in a 32bit microcontroller. The analog part of the CDC that we propose is only composed of a voltage down converter, current mirror circuit, and current-controlled oscillator. Since its analog part is so simple that our CDC can be easily ported to various kinds of processes with which microcontrollers are fabricated. RF noise immunity of our CDC is enhanced by using the random phase shift scheme that we developed. The effectiveness of the scheme was experimentally verified with a CDC integrated in a 32bit microcontroller which was fabricated in 130nm CMOS process. Our CDC meets level 3 of IEC 61000-4-3 and IEC 61000-4-6 standards. With our CDC structure, users can select resolution under a trade-off between the resolution and measurement time. If the measurement time is extended up to 50ms, its resolution is as high as 2aF. 3D gesture sensing was realized using the 32bit microcontroller in which the proposed CDC was integrated.

Keywords: capacitive sensor, capacitance-to-digital converter, noise immunity, microcontroller, gesture sensing

20-2

4:15 PM - 4:40 PM

A 104.8TOPS/W One-Shot Time-Based Neuromorphic Chip Employing Dynamic Threshold Error Correction in 65nm

Luke Everson, Muqing Liu, Nakul Pande, Chris Kim

University of Minnesota, United States

Abstract:

We propose a time-domain core using one-shot delay measurements and a lightweight post-processing technique, Dynamic Threshold Error Correction (DTEC). This design differs from traditional digital implementations in that it uses the delay accumulated through a simple inverter chain distributed through an SRAM array to intrinsically compute resource intensive multiply-accumulate (MAC) operations. Implemented in 65nmLP CMOS we achieve, to our knowledge, the lowest reported energy efficiency for a neuromorphic processor with 52.4TSOp/s/W (104.8TOp/S/W) at 0.7V with 3b resolution for an impressive 19.1fJ/MAC.

Keywords: Neuromorphic, Time Domain Neural Network, TDNN, Deep Learning

20-3 (Short Paper)

4:40 PM - 4:52 PM

A 137- μ W Area-Efficient Real-Time Gesture Recognition System for Smart Wearable Devices

Taegeun Yoo², Van Loi Le², Ju Eon Kim¹, Ngoc Le Ba², Kwang-Hyun Baek¹, Tony Tae-Hyoung Kim²

¹Chung-Ang University, Korea; ²Nanyang Technological University, Singapore

Abstract:

Gesture recognition has increasingly become one of the most popular human-machine interaction techniques for smart devices. Existing gesture recognition systems suffer from either excessive power consumption or large size, limiting their applications for ultra-low power IoT and wearable devices. This paper presents an accurate, area-efficient, and ultra-low power real-time gesture recognition system for smart wearable devices. The proposed work utilizes a peak-based gesture classification engine with less memory and a low-resolution and low-power on-chip image sensor for achieving high area efficiency and low power. The feature extraction architecture removes fixed-pattern noises from the low-power on-chip image sensor for accuracy improvement and employs parallelism for recognition speed enhancement. The proposed system requires only 3.2 KB on-chip memory for processing 32 \times 32 pixel data. Measurement results of a test chip fabricated in 65nm CMOS demonstrate that the proposed system consumes 137.0 μ W at 0.8 V and 30fps while occupying only 1.78mm², which achieves the lowest power and smallest area among existing gesture recognition systems.

Keywords: gesture recognition, system on chip, feature extraction, low power processor, image sensor, wearable devices

20-4 (Short Paper)

4:52 PM - 5:05 PM

A 655Mbps Successive-Cancellation Decoder for a 1024-Bit Polar Code in 180nm CMOS

Hye-Yeon Yoon, Seung-Jun Hwang, Tae-Hwan Kim

Korea Aerospace University, Korea

Abstract:

This paper presents the implementation of a high-throughput successive-cancellation decoder for a 1024-bit polar code. The proposed decoder processes the kernels in two successive layers in a fused manner within a cycle, so as to reduce the cycle count taken to decode a codeword. In addition, the log-likelihood ratios are represented in a redundant form to realize a high-speed kernel processing. As a result, the cycle period is not lengthened even with the fused kernel processing and thus achieving a high throughput. Implemented in 180nm CMOS, the proposed decoder shows the throughput of 655 Mbps for the rate-1/2 code. In terms of the throughput efficiency, the proposed decoder is 3.51 times superior to the previous state-of-the-art one.

Keywords: Polar code, successive cancellation decoding, high throughput, error-correcting code.

A Generated Multirate Signal Analysis RISC-V SoC in 16nm FinFET

Stevo Bailey, Jaeduk Han, Paul Rigge, Richard Lin, Eric Chang, Howard Mao, Zhongkai Wang, Chick Markley, Adam Izraelevitz, Angie Wang, Jonathan Bachrach, Elad Alon, Borivoje Nikolic
UC Berkeley, United States

Abstract:

This paper demonstrates a signal analysis SoC consisting of a general-purpose RISC-V core with vector extensions and a fixed-function signal-processing accelerator. Both the core and the accelerators are instances produced by generators that allow for a wide range of parameter configurations and rapid design space exploration. The signal processing chain consists of generated instances of a time-interleaved ADC followed by a digital tuner, FIR filter, polyphase filter, and FFT all connected to the processor via an AXI4 bus. The 5mmx5mm chip is implemented in a 16nm FinFET process and operates at 410MHz at 750mV drawing 600mW. Presented applications show coupled functionality of the processor and accelerator performing spectrometry and radar receive processing, and a comparison with other state-of-the-art ASICs prove that generators can produce competitive designs.

Keywords: DSP, Generators, RISCV, FinFET, Radar, Spectrometer, Signal Analysis, Vector, DMA

Session	RF 21: Low-Power RF Transmitters and Receivers
Date / Time	November 7, 2018 (Wednesday) / 3:50 PM - 5:30 PM
Room	East Gate, B1F
Chair	Taizo Yamawaki, Hitachi
Co-Chair	Chien-Nan Kuo, National Chiao Tung University

21-1

3:50 PM - 4:15 PM

A Compact High Efficiency and High Power Front-End Module for GSM EDGE TD-SCDMA TD-LTE Applications in 0.13um CMOS

Shihai He, Fengxiong Peng, Linjian Xu, Hao Meng, Yongxue Qian
Beijing Huntersun Electronic Co.,Ltd., China

Abstract:

This work presents a fully integrated multimode multiband transmitter front-end module (TXM) supporting GSM/EDGE/TD-SCDMA/TDD-LTE application. The TXM including the 0.13um CMOS PA, SP16T antenna switch and all passive components is fully integrated in a flip-chip LGA package. It achieves 30dBm at 915 MHz, 27dBm at 1910 MHz with -35/-61dBc ACLR1/2 in EDGE mode. It also supports 27dBm Pout(-40/-61dBc ACLR1/2) in TD-SCDMA mode and 24dBm Pout(-36dBc EUTRA) in TD-LTE mode. This work presents a completed solution for multimode multiband TXM with very low cost, high output power and high efficiency.

Keywords: CMOS, power amplifier, flip-chip, front-end module, transformer, EDGE, wireless communication

21-2

4:15 PM - 4:40 PM

A 2.4-GHz Single-Pin Antenna Interface RF Front-End with a Function-Reuse Single-MOS VCO-PA and a Push-Pull LNA

Kai Xu¹, Jun Yin², Pui-In Mak², Robert Bogdan Staszewski¹, Rui P. Martins²
¹University College Dublin, Ireland; ²University of Macau, China

Abstract:

We introduce a power-efficient sub-1V RF front-end (RFE) for 2.4GHz transceivers. It features the following innovations: 1) function-reuse single-MOS VCO-PA with low voltage headroom while improving antenna-to-VCO isolation for better resilience to jammers; 2) a non-inverting transformer with a zero-shifting capacitor that suppresses the 2nd harmonic emission of the VCO-PA, and allows a single-pin antenna interface for both transmitter and receiver modes, and 3) a push-pull LNA with passive gain boosting that reduces power consumption. Fabricated in 65nm CMOS, the RFE occupies a small die area of 0.17mm². By scaling the supply voltage, the standalone VCO-PA exhibits a 20.8% (10.2%) power efficiency when delivering 0dBm (-10dBm) output. The LNA shows 11dB gain and 6.8dB NF while consuming 174μW.

Keywords: RF Front-end, VCO-PA, LNA and single-pin antenna interface

21-3 (Short Paper)**4:40 PM - 4:52 PM****A 6-8GHz 200MHz Bandwidth 9-Channel VWB Transceiver with 8 Frequency-Hopping Sub-Bands**

Haixin Song, Dang Liu, Woogeun Rhee, Zhihua Wang

*Institute of Microelectronics, China***Abstract:**

This paper presents a pulse-based OOK transceiver system which enables up to 9-channel transmission over 6-8GHz frequency band for the first time. Having eight frequency-hopping subbands, a very-wideband (VWB) transceiver achieves a 200MHz bandwidth with steep spectral roll-off and complies with ultra-wideband (UWB) emission mask. The VWB transmission with 1-64ns pulse duration offers a flexible communication range and a relaxed pulse generation circuit design in the transmitter. In the receiver, an asynchronous energy detection (AED) method which does not require multiphase clock generation is employed. The proposed VWB transceiver implemented in 65nm CMOS consumes 0.81mW with 20ns pulse duration at 1Mb/s data rate.

Keywords: VWB, spectral efficiency, asynchronous noncoherent demodulation, multiple channels

21-4 (Short Paper)**4:52 PM - 5:05 PM****A 0.46-2.1GHz Spurious and Oscillator-Pulling Free Lo Generator for Cellular NB-IoT Transmitter with 23 dBm Integrated PAs in 28nm CMOS**

Jaewon Choi, Nam-Seog Kim, Juyoung Han, Thomas B. Cho

*Samsung Electronics, Korea***Abstract:**

This paper presents a spurious/pulling free LO generator (LOG) using reconfigurable of divider-2 and mixed-mode fractional divider-by-2.5 to mitigate the DCO pulling from integrated power amplifier for a cellular NB-IoT application. The divider ratio in the designed LOG is determined by TX output power level to achieve both the mitigation of pulling and effective current consumption. Adaptive voltage bias (ADB) circuit is added to compensate PVT variation for the fractional divider. A proposed reconfigurable LOG is implemented in 28nm CMOS process and it consumes 40mA including ADPLL, DCO and dividers. The measured phase noise of the 2GHz carrier LOG with Div2.5 is -146.3dBc/Hz at 10MHz offset. Fractional spurs are below than -90 dBc without pulling for 1.6~2.1GHz output frequency

Keywords: Reconfigurable of LOG, Mixed-mode Fractional Divider, Cellular NB-IoT, Integrated PA, Pulling Mitigation, Spurious Free

21-5**5:05 PM - 5:30 PM****A 152μW -99dBm BPSK/16-QAM OFDM Receiver for LPWAN Applications**

Avish Kosari, Milad Moosavifar, David Wentzloff

*University of Michigan, United States***Abstract:**

This paper presents a 152μW BPSK/16-QAM OFDM receiver operating in the 151MHz Multi-Use Radio Service (MURS) frequency band for low power and long-range IoT applications. Sub-harmonic passive mixers and an injection locked ring oscillator are used, together with a dual-IF architecture for power efficiency and blocker rejection. As a solution for LPWAN applications, the receiver is designed to operate

in two modes of single-carrier and multi-carrier transmission schemes, and is implemented in a 40nm CMOS process consuming 152 μ W of power while achieving a sensitivity of -99dBm for BPSK modulation at 5kb/s and -77dBm for 16-QAM OFDM modulation at 384kb/s. Under only 0.9V of supply, it achieves a phase noise of -128dBc/Hz at 1MHz offset, a blocker rejection of 63dB, and is fully integrated except for the reference crystal and the balun.

Keywords: Injection locking, IoT, long-range, low power radios, LPWAN, MURS band, sub-harmonic mixing.