# Call for Papers

## IEEE Asian Solid-State Circuits Conference

## A-SSCC 2018

**Location: Shangri-La's Far Eastern Plaza Hotel, Tainan, Taiwan**

**Date: November 5 – 7, 2018**

Sponsored by IEEE SSCS, IEEE Region-10 SSCS Chapters

http://www.asscc.org

http://sscs.ieee.org

**Conference Theme: Silicon Enabling Mobile Intelligence**

The miniaturized silicon technology enabled big success in the realization of software solutions such as machine learning, big data, virtual and augmented realty in the image and speech recognition, the medical diagnosis and the autonomous driving automobiles. The current software solutions, however, consume huge power by employing cloud computers along with many graphic processing units and a large amount of memory. Nowadays, the integrated circuit design community tries to develop efficient low-power mobile intelligence solutions by taking challenges in the design of digital and analog circuits, processor architecture, and system for compact IoT devices.

The IEEE A-SSCC 2018 (Asian Solid-State Circuits Conference) is an international forum for presenting the most updated and advanced chips and circuit designs in solid-state and semiconductor fields. The conference is supported by the IEEE Solid-State Circuits Society and will be held in Asia. Further details on the conference and paper submission guidelines and templates will be available at the A-SSCC official website http://www.asscc.org (or http://www.a-sscc2018.org/) around the beginning of April 2018.

### Paper Submission

1. Prospective authors are invited to submit **four-page or two-page (NEW)** manuscripts, including figures, tables and references, to the official A-SSCC 2018 website. **The two-page submission could include two-page supplements with figures and figure captions.** All papers will be handled and reviewed electronically. Papers are solicited in the following categories:

### Regular Session

1. **Analog Circuits & Systems:** Amplifiers, comparators, switched capacitor circuits, continuous-time & discrete-time filters, voltage/current references; DC-DC converters, power-control circuits; IF/baseband analog circuits, AGC/VGA; non-linear analog circuits.
2. **Data Converters**: Nyquist-rate and oversampling A/D and D/A converters, time-to-digital converters, and capacitance-to-digital converters; sub-circuits for data converters including sample-and-hold circuits, calibration circuits, etc.
3. **Digital Circuits & Systems:** Design, fabrication, and test of digital VLSI systems; high-speed low-power digital circuits, power-reduction and management methods for digital VLSI, ultra-low-voltage and sub-threshold logic design; leakage reduction techniques; clock distribution, I/O circuits, reconfigurable logic-array circuits; supply/substrate noise measurement and cancellation for digital VLSI, variation and fault-tolerant circuits.
4. **SoC & Signal Processing Systems: System-on-chip(including 3D integration), microprocessors, network processors, baseband communication processing system & architectures, system-level power management; multimedia and recognition processing systems; cryptographic, security, machine-learning, deep-learning, and neuromorphic circuits and systems; bio-medical/neural-network processors and sensor network systems.**
5. **RF:** Receivers/transmitters/transceivers for wireless systems; narrowband RF, ultra-wideband and millimeter-wave circuits; circuits and building-blocks including RF front-end, LNA, mixer, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, active antennas.
6. **Wireline:** Receivers/transmitters/transceivers for wireline systems; optical/electrical data links and backplane transceivers; power-line communication; clock generation circuits, PLL, DLL, spread-spectrum clock generation; building blocks for high-speed wireline communication; analog-digital mixed-mode circuits.
7. **Emerging Technologies and Applications:** Advanced system designs and circuit solutions for technologies and applications including state-of-the-art devices and packaging technologies; flexible and printable electronics; smart sensors and transducers; MEMS for analog, RF, and sensor applications; image sensors and displays; energy harvesting systems; transceiver systems; medical/bio-electronics/bio-inspired chip design and silicon systems.
8. **Memory: Volatile and Non-volatile memory; new memory designs for 3D/2D architectures, emerging devices such as resistive-/phase change-/magnetic-/ferro-electric- memory devices; data storage and multi-bit-cell memory design; cache-memory system, multi-port memory, memory subsystem, processing in memory, and CAM design; yield-enhancing and ECC techniques; memory testing and built-in self-test.**

### Special Session

1. **Industry Program:** This special category accepts only papers based on state-of-the-art industrial products. Strong emphasis on systems realized by silicon chips is encouraged. The papers should cover architecture, circuits, process technology, packaging and testing, including characterization results, die and system photos, as well as product demos.
2. **Student Design Contest:** A student design contest is held among the accepted papers with system prototypes or measurement results of which operations can be demonstrated on-site. Refer to the web for further information.
3. **FPGA Session (NEW) : This session accepts papers describing FPGA implementation with novel algorithm and/or architecture. The demo results(eg. video or slide) must be included in the paper submission. The authors of accepted papers are required to participate in demo sessions.**

Papers related to integrated circuits for intelligent systems are highly solicited. Papers on low-power and/or low-voltage approaches, signal integrity, noise, test, and manufacturability for all the above categories are welcomed. Measurement results are highly recommended, especially for analog, and RF categories. Design methodologies for SiP, and SoC are included in the scope of the conference; the papers only describing CAD tools and CAD algorithms are not considered. Authors must follow detailed instructions provided within the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy. The technical content beyond the abstract of the accepted paper must not be announced, published, or in any way put in the public domain prior to the Conference. Extended versions of selected papers from the Conference will be published in a **Special Issue of the IEEE Journal of Solid-State Circuits**.

**Important dates**

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| **Paper submission** | **June 3, 2018, 23:59 (GMT -0700)** | **Acceptance notification** | **August 6, 2018** |
| **Final paper submission** | **September 9, 2018** | | |

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